

INTERFACE

45C

MICROCOMPUTING FOR HOME AND SMALL BUSINESS VOL. 2, ISSUE 2 JAN. 1977

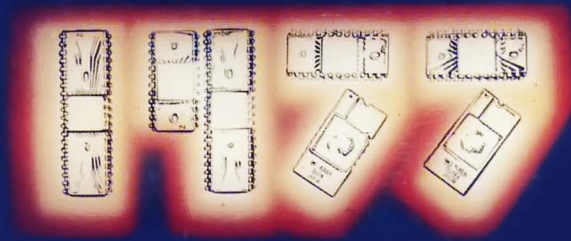
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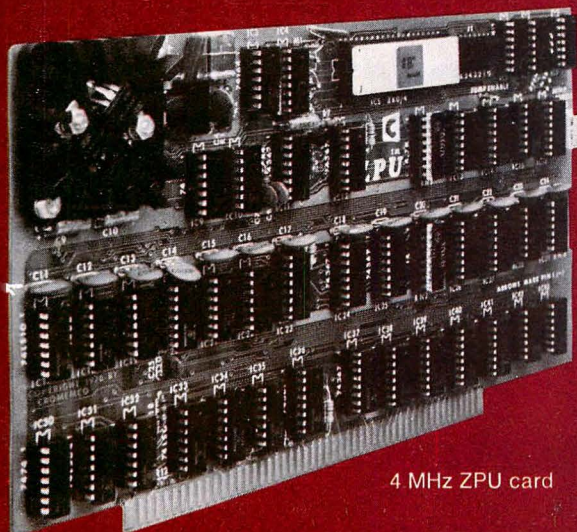
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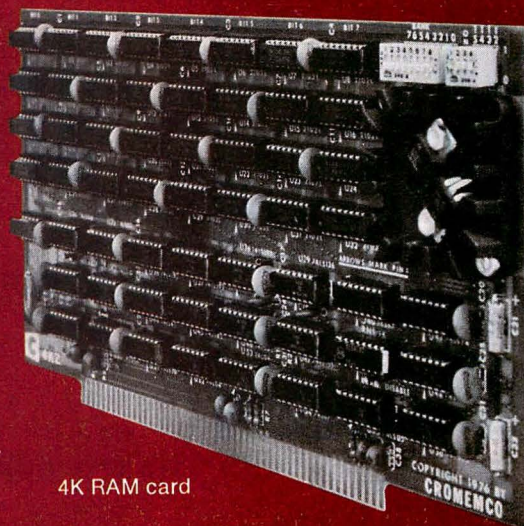
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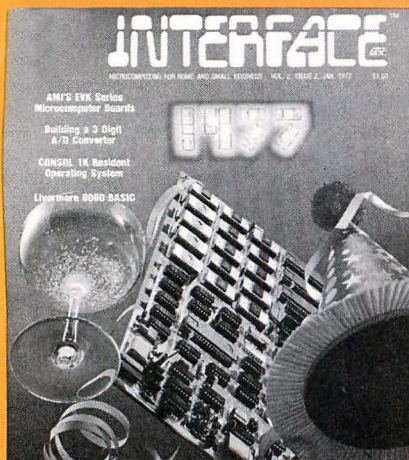
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CIRCLE INQUIRY NO. 8



INTERFACETM

MICROCOMPUTING FOR HOME AND SMALL BUSINESS

Cover Story

Almost daily the microcomputer industry celebrates new advances as more and more creative and ingenious ideas are turned into state-of-the-art products.

Because of the increasing versatility enabled by the wide breadth of low-cost peripherals, today's user can now approach a fairly sophisticated microcomputer system and maintain financial solvency. This month's feature, "AMI's EVK Series Microcomputer" is the story of just one such microcomputer whereby a standard prototype board becomes the common vehicle for four configurations based on the user's memory and application needs.

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One of the first things you'll discover when you get started with microprocessors is that there's a lot more involved than the hardware. That's why you should consider a system's software, too.

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Every system the Digital Group delivers has several operating programs included with it. As soon as you turn it on it's doing something! In addition, we make available an ever-growing number of software packages for Digital Group systems at all levels of support. (They're listed below.)

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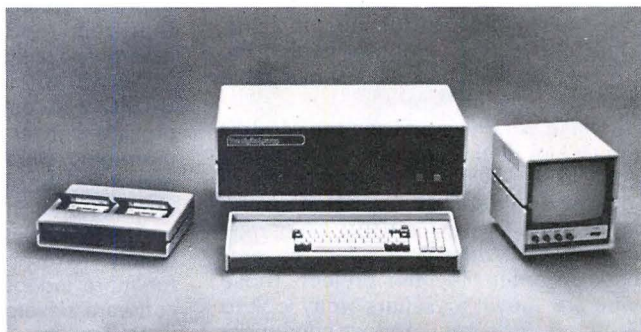
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INTERFACIAL



The beginning of the new year finds both consumer and manufacturer with high expectations for a very dynamic market place. Semiconductor manufacturers are readying to launch their new microcomputers into the arena such as Intel's 8085 (single supply, micro system on a chip), Fairchild's new microcomputer system on a card and Motorola's new microcomputer HEP kit.

The message seems to be coming through loud and clear as most of the new entries from the manufacturers are aimed at the low cost market place with improved performance over their more costly ancestors.

To start your microcomputing year off with a sizzling success we have compiled a bonanza of indepth hardware and software entries which we expect you will find as an invaluable addition to your library.

Those who have utilized the M6800 family in their personal computing applications, will find the first article of interest as a detailed discussion involving a CRT Controller application may inspire the "do-it-yourselfer" to embark on another winter project. Those who are "buy it myselfers" may look to Motorola for a new product announcement. Nevertheless Joe Roy and Dusty Morris have offered a good insight into what it takes.

Part II of a four part series on AMI's Microcomputers cover the EVK Prototype card architecture and a comparative analysis of each of the four basic configurations offered.

"Building a 3 digit A/D converter" can not only be a challenging job but can be fun if most of the toil is removed by virtue of a single chip. Roger Edelson explores the Siliconix LD130 bi polar A/D chip and applications in a microcomputer with a two part series starting this month.

Terry Benson, Field Applications Engineer for Intel Corp, turns his prolific pen loose on "Microcomputer Design Aides." A bit of a squint is pro-

vided for another new tool, the PROMPT 80™ a self contained micro-computer development system which supports the design of any 8080 system. The PROMPT 80™ is reputedly a personal programming tool as well as a professional's programming delight.

The "Card-of-the-Month" feature is a mind soother and program expeditor. Around for awhile and still in great demand, the Cromemco BYTESAVER™ is reviewed with a lusty zeal as our hardware editor pokes and prys at its features and tests its performance.

A resident 8080 software package, "CONSOL" developed by Processor Technology for their new Intelligent Microcomputer Terminal called SOL is featured including the complete assembly listing.

Two BASIC interpreters, one on Tiny BASIC and one on standard BASIC provide conversational language programming capabilities for the SC/MP and 8080 based Microcomputers are also featured in this issue.

The features in this month's issue are chiefly in response to many requests for more indepth product reviews and software development programs.

Remember we try to be responsive to your needs and the only way we can succeed is through your continued communication. Feel free to drop us a line and tell us what you would like to see in future issues.

If you have composed an article on a subject you feel others would be interested in, let us take a look at it. If we concur, we will publish it and that also means it could make you some money — as well as satisfy that creative pen.

INTERFACE AGE will pay up to \$50 per published page as well as award each monthly "best article" author an additional \$100.00. The annual "best article" award is \$500 in cash or equipment.

Editor

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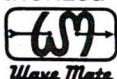
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Update

NOTABLES

"Who are we?" "How did we get here?" "Are we alone in the Universe?" The answers to these questions have broad scientific implications, as well as deep philosophical, sociological, and theological meaning. The search for extraterrestrial intelligence has begun!

The Forum for the Advancement of Students in Science and Technology (FASST), the Student Programs Division of the American Institute of Aeronautics and Astronautics (AIAA), and the Educational Programs Office of the NASA/Ames Research Center, invite you to take part in the search by participating in a special symposium,

"The Search for Extraterrestrial Intelligence (SETI)." The program will be held at the Ames Research Center, near San Francisco, on February 24-25, 1977.

Speakers and participant discussion groups will cover such topics as: "The Cosmic Picture — Is Anyone Really Out There?"; "The Origin of Life — Chemical and Biological Considerations"; "Evolution of Technological Civilizations"; "Methods and Technology for the Search"; and "Cultural Implications of Detection and Contact with Extraterrestrial Intelligence."

Confirmed speakers for the symposium include Dr. Richard Berendzen, astronomer, lecturer, author and Chairman for the Boston SETI sym-

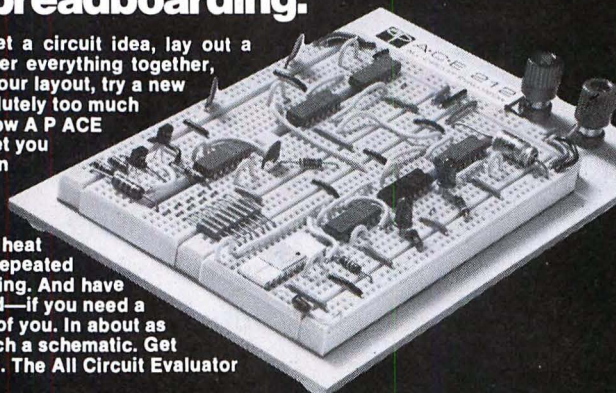
posium, "Life in the Mind of Man"; Dr. John Billingham, Chief, Program Office for SETI-NASA/Ames; Ronald Bracewell, Professor/Stamford University and author of THE GALACTIC CLUB; David Black, Project scientist/SETI; Dr. James Christian, philosopher and author of EXTRATERRESTRIAL INTELLIGENCE: The First Encounter; and Bernard Oliver, Vice President for Research, Hewlett-Packard, and formerly Director of the study group on constructing large arrays of radio telescopes, designated Project Cyclops. We are awaiting confirmation of Dr. Carl Sagan, astronomer/biologist, and Dr. Stanley Miller, biochemist.

Directed, primarily, toward college and university students, the symposium also welcomes participation by interested professionals and faculty members. A wide cross section of academic disciplines will be involved, including students in anthropology, theology, life science, engineering, sociology, etc.

Registration fee for the conference is \$10.00, which includes symposium materials, a tour of the Ames facilities, and a banquet. The grant to conduct this program did not include funds for student travel. For those who would like to participate but live outside the San Francisco area, we recommend that you seek financial assistance locally from your academic department or campus student activity fund. In your request for funding, include a statement on how the conference applies to your educational objectives, and the benefits to be derived from attending. FASST will send support letters upon your request. Requests may be addressed to FASST, 1785 Massachusetts Avenue, N.W., Washington, D.C. 20036. Telephone (202) 483-2900.

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923334	201-K (kit)	1032	12 (14's)	2	2	4-9/16x7	24.95
923331	212 (assem.)	1224	12 (14's)	8	2	4-9/16x7	34.95
923326	218 (assem.)	1760	18 (14's)	10	2	6-1/2x7-1/8	46.95
923325	227 (assem.)	2712	27 (14's)	28	4	8x9-1/4	59.95
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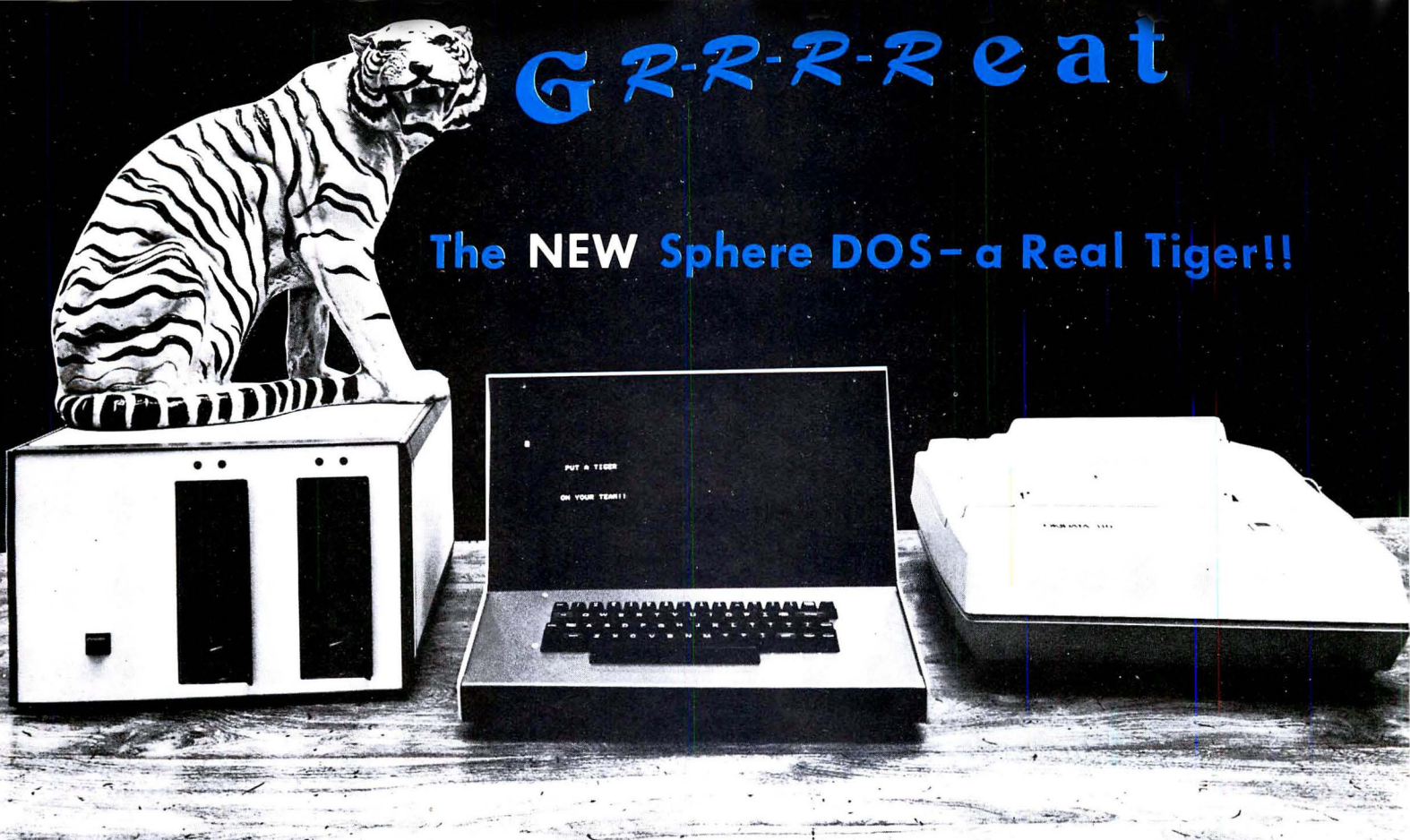
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- deal with multiple devices of several types
- operate on both our 300 and 500 systems.

So, we designed the all-new Sphere DOS, and we have a lot of good reasons for calling it a tiger! It is a truly remarkable DOS . . . worth checking into. Once you do, we think you'll find it easy to make the decision to

PUT THIS TIGER ON YOUR TEAM!!!

DOS SPECIFICATIONS

LANGUAGE	Motorola M6800 Assembler
STORAGE REQUIREMENT	5K Bytes
OPERATING ENVIRONMENT	Sphere 300 and 500 Series Systems
CONVENIENCE PROGRAMS PROVIDED	Editor, Debugger, Assembler, Set of File-manipulating Commands (macro-like operations)
PERIPHERALS SUPPORTED STRUCTURE	CRT, Keyboard, Floppy Disk Drive, TTY Uniform, interrupt-driven I/O

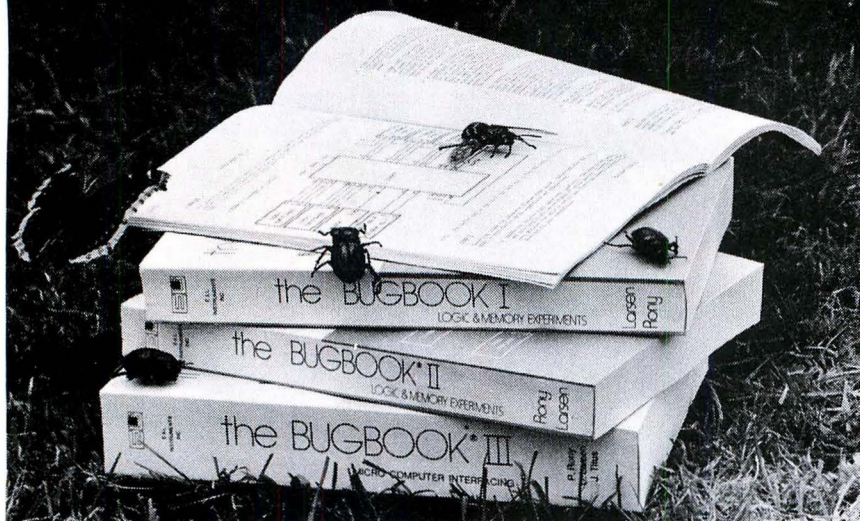
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CIRCLE INQUIRY NO. 11

developing new games and applications."

Both stores conduct introductory classes and provide free in-store lectures for schools and civic groups. The owners feel that increasing public awareness of the potential for personal computing is a major part of their business. They both have been active in speaking to local organizations about the future and microcomputing. Both owners are looking forward to bringing the fun and capability of personal computing to Arizonans.

For further information contact either Alan or Jeffry at (602) 894-1129 or (602) 942-7300.

CALL FOR PAPERS

The UPIEEE-77 Workshop (June 1977) "On Beach Programming of Microprocessors" is soliciting papers from people who have incorporated microprocessors into a product without the use of expensive MP program development equipment. Three types of papers are expected — software, hardware and trouble-shooting (debugging). All hardware papers accompanied by a working board will be published in the Proceedings.

In the 1950s the physicists gave us the transistor. Before we could conveniently use it in circuit design, we

had to strip it of the theory with which the physicists had saddled it, and provide it with a practical engineering approach. Now the computer people have given us the microprocessor. Before we can conveniently use it, we have to strip it of the top-heavy computer approach and provide it with a practical engineering approach for use in circuit design.

The purpose of the μ PIEEE-77 workshop is to exchange experiences and learn pitfalls and shortcuts in writing firmware; and in trading-off firmware, software and hardware right at the design bench. Papers are due before February 1.

The workshop will take place on Friday, Saturday and Sunday, June 10, 11 and 12, in Philadelphia. Dormitory space will be available to out-of-town participants. Proceedings will be published beforehand and mailed to participants. There will be no reading of papers — only discussion, questions and answers, and demonstration of boards. Boards chosen for publication only will be displayed in the lobby, and authors will be given time for poster talks. Time will be allocated for bull sessions.

For further information about μ PIEEE-77 contact Miss Helen B. Yonan, Philadelphia IEEE, Moore School, University of Pennsylvania, Philadelphia, PA 19174.

TENTH ONE-DAY TECHNICAL SYMPOSIUM

The Los Angeles Chapter of the Association for Computing Machinery has announced final arrangements for its Tenth One-Day Technical Symposium.

Date: February 4, 1977.

Location: Hoffman Hall, University of Southern California, Los Angeles.

Theme: Computers . . . the Continuing Revolution.

Registration Fee: Early - \$15.00, Late - \$20.00. Fee covers programs and lunch.

Morning Program: Software, the new emphasis.

Speakers and their subjects will be Dr. Robert Brown, Hughes Aircraft Company, "Principle Aspects of Structured Design"; Dr. Jack Holton, University of Southern California, "Modern Techniques for Programming System Development — Are They Useful?"; Guy de Balbine, Caine Farber Gordon, Inc., "An Assessment of Structured Processor Technology: Present and Future"; Prof. Brinch Hansen, University of Southern California, "The Underlying Architecture of the Concurrent PASCAL Machine."

The lunch will be a complete steak dinner. Luncheon speaker will be Victor Azgabetian, Aerojet General, "A Look Into the Future From the Wrong Point of View."

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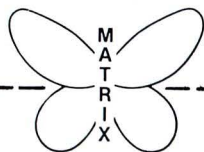
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CIRCLE INQUIRY NO. 17

Afternoon Program: Hardware, the micro revolution. Speaking will be Ron Muir, ROM Systems, "Emulation Utilizing the 2900 Microprocessor Bit Slice Chip Set"; Elizabeth Rather, Forth, Inc., "FORTH as a Programming Support System for Microprocessor"; and Les Lazar, Digital Design and Development, "Cost Versus Performance Tradeoffs for Several Microprocessors."

PANHANDLE COMPUTER SOCIETY AMARILLO, TEXAS

The Texas Panhandle now has a computer hobbiest club and though less than 3 months old, we boast a membership of more than 30.

The Panhandle Computer Society meets every Friday and is open to anyone interested in computers. We also welcome replies from other groups, especially in Texas.

Those interested may contact the president, Tex Everett, 2923 S. Spring, Amarillo, Texas 79103 (Phone: 806-373-8207) or the secretary/treasurer: Jerry Fewell, 3109 Browning, Amarillo, Texas 79103 (phone 806-374-0897).

CALENDAR

Jan. 3 South Florida Computer Group, Miami Division meets at 7:30 p.m., PAP Institute, 1155 NW 14th St., Miami, FL. General Meeting. For more information call (305) 271-2805.

Jan. 4 El Paso Computer Group meets at 7:00 p.m., Meeting place information call (915) 544-1542.

Jan. 5 Northwest Computer Club meets at 7:00 p.m., Pacific Science Center, Seattle, WA. Informal Meeting. Details by calling (206) 524-6359.

Jan. 5 New England Computer Society, Inc. meets at 7:00 p.m., MITRE Corp. cafeteria, Route 62, Bedford, MA. For further information call Dave Day (603) 434-4239.

Jan. 5 Southern California Computer Society Valley Chapter meets at 7:00 p.m., Harvard School, 3700 Cold Water Canyon, Studio City, CA. Technical session on the TI-9900 Microprocessor by a representative of Texas Instruments Co. Call John Scott at (213) 849-4094 for further details.

Jan. 8 The Permian Basin Computer Group, Midland Chapter meets at 4:00 p.m., Midland College, Occupational Technology Bldg., Room 110. More details call (915) 697-4607.

Jan. 8 The Permian Basin Computer Group, Odessa Chapter meets at 1:00 p.m., Odessa College, Electronics Technology Bldg., room 203. Please call (915) 332-9151 for further details.

Jan. 8 Louisville Area Computer Club meets at 1:00 p.m., Speed Auditorium, University of Louisville. General meeting. Contact Glen Darwin (502) 456-5589 or by writing at 3028 Hunsinger Ln., Louisville, KY 40200.

Jan. 9 Southern California Computer Society, Orange County Chapter meets at 12:00 noon, California State University, Fullerton, Administration Bldg., Room 321. For meeting agenda call: Lorin Mohler at (714) 998-5831.

Jan. 9 University of Chicago Computer Club meets at 1:00 p.m., Reynolds Club, 57th and University, Chicago, IL. For more information call (312) 421-0244.

Jan. 9 Oklahoma Computer Club meets at 10:00 a.m., Bell Aisle Library, Oklahoma City, OK. General Meeting. Call Al Campbell (405) 842-4933.

Jan. 13 Rochester Area Microcomputer Society meets at 6:30 p.m., Room 1030, Bldg. 9, Rochester Institute of Technology, Rochester, NY. Meeting will feature William Mathis and the inside scoop on the KIM-1. Mailing address, RAMS, P.O. Box D, Rochester, NY 14609.

Jan. 14 Crescent City Computer Club meets at 8:00 p.m., University of New Orleans, Lakefront Campus. Contact Bob Latham (504) 722-6321 or P.O. Box 1097, New Orleans, LA 70122.

Jan. 15 South Central Kansas Amateur Computer Association meets at 9:00 a.m., 1430 E. Kellogg (next to Church of the Nazarene). Call Cris Borger at (316) 945-9658 for more information.

Jan. 15 So. Cal. SWTPCO MP 6800 Users Group meets at A-VID Electronics, 1655 E. 28th Street, Long Beach, CA 90806 at 10:00 a.m.

Jan. 19 Denver Amateur Computer Society DACS meets at 7:30 p.m., 4101 E. Hampden Av. Denver, CO. General Meeting. Call (303) 333-1047.

Apple Introduces the First Low Cost Microcomputer System with Video Terminal and 8K Bytes of RAM on a Single PC Card.

The Apple Computer. A truly complete microcomputer system on a single PC board. Based on the MOS Technology 6502 microprocessor, the Apple also has a built-in video terminal and sockets for 8K bytes of on-board RAM memory. With the addition of a keyboard and video monitor, you'll have an extremely powerful computer system that can be used for anything from developing programs to playing games or running BASIC.

Combining the computer, video terminal and dynamic memory on a single board has resulted in a large reduction in chip count, which means more reliability and lowered cost. Since the Apple comes fully assembled, tested & burned-in and has a complete power supply on-board, initial set-up is essentially "hassle free" and you can be running within minutes. At \$666.66 (including 4K bytes RAM!) it opens many new possibilities for users and systems manufacturers.

You Don't Need an Expensive Teletype.

Using the built-in video terminal and keyboard interface, you avoid all the expense, noise and maintenance associated with a teletype. And the Apple video terminal is six times faster than a teletype, which means more throughput and less waiting. The Apple connects directly to a video monitor (or home TV with an inexpensive RF modulator) and displays 960 easy to read characters in 24 rows of 40 characters per line with automatic scrolling. The video display section contains its own 1K bytes of memory, so all the RAM memory is available for user programs. And the

Keyboard Interface lets you use almost any ASCII-encoded keyboard.

The Apple Computer makes it possible for many people with limited budgets to step up to a video terminal as an I/O device for their computer.

No More Switches, No More Lights.

Compared to switches and LED's, a video terminal can display vast amounts of information simultaneously. The Apple video terminal can display the contents of 192 memory locations at once on the screen. And the firmware in PROMS enables you to enter, display and debug programs (all in hex) from the keyboard, rendering a front panel unnecessary. The firmware also allows your programs to print characters on the display, and since you'll be looking at letters and numbers instead of just LED's, the door is open to all kinds of alphanumeric software (i.e., Games and BASIC).

8K Bytes RAM in 16 Chips!

The Apple Computer uses the new 16-pin 4K dynamic memory chips. They are faster and take 1/4 the space and power of even the low power 2102's (the memory chip that everyone else uses). That means 8K bytes in sixteen chips. It also means no more 28 amp power supplies.

The system is fully expandable to 65K via an edge connector which carries both the address and data busses, power supplies and all timing signals. All dynamic memory refreshing for both on and off-board memory is done automatically. Also, the Apple Computer can be upgraded to use the 16K chips when they become availa-

ble. That's 32K bytes on-board RAM in 16 IC's—the equivalent of 256 2102's!

A Little Cassette Board That Works!

Unlike many other cassette boards on the marketplace, ours works every time. It plugs directly into the upright connector on the main board and stands only 2" tall. And since it is very fast (1500 bits per second), you can read or write 4K bytes in about 20 seconds. All timing is done in software, which results in crystal-controlled accuracy and uniformity from unit to unit.

Unlike some other cassette interfaces which require an expensive tape recorder, the Apple Cassette Interface works reliably with almost any audio-grade cassette recorder.

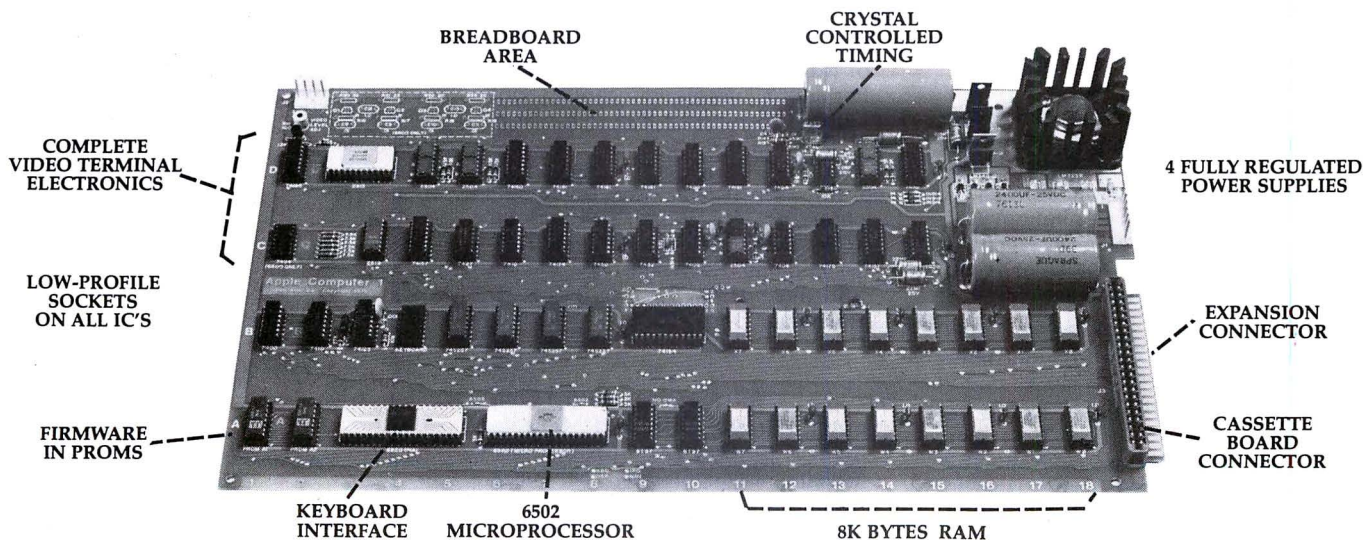
Software:

A tape of APPLE BASIC is included free with the Cassette Interface. Apple Basic features immediate error messages and fast execution, and lets you program in a higher level language immediately and without added cost. Also available **now** are a dis-assembler and many games, with many software packages, (including a macro assembler) in the works. And since our philosophy is to provide software for our machines free or at minimal cost, you won't be continually paying for access to this growing software library.

The Apple Computer is in stock at almost all major computer stores. (If your local computer store doesn't carry our products, encourage them or write us direct). **Dealer inquiries invited.**

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*includes 4K bytes RAM



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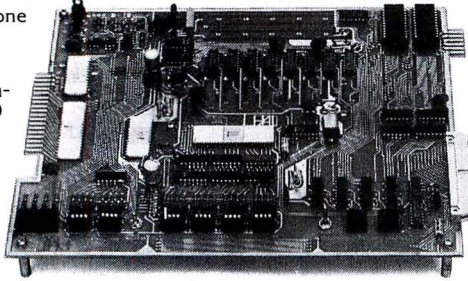
JANUARY 1977

CIRCLE INQUIRY NO. 2

INTERFACE AGE 11

If you want a microcomputer with all of these standard features...

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- 3 parallel I/O's
- ASCII/Baudot terminal compatibility with TTY machines or video units
- Monitor having load, dump, display, insert and go functions



- Complete with card connectors
- Comprehensive User's Manual, plus Intel 8080 User's Manual
- Completely factory assembled and tested—not a kit
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HAL Communications Corp. has been a leader in digital communications for over half a decade. The MCEM-8080 microcomputer shows just how far this leadership has taken us...and how far it can take you in your applications. That's why we'd like to send you our card—one PC board that we feel is the best-valued, most complete



microcomputer you can buy. For details on the MCEM-8080, write today. We'll also include comprehensive information on the HAL DS-3000 KSR microprocessor-based terminal, the terminal that gives you multi-code compatibility, flexibility for future changes, editing, and a convenient, large video display format.

HAL Communications Corp.

Box 365, 807 E. Green Street, Urbana, Illinois 61801
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CIRCLE INQUIRY NO. 17

Jan. 19 Northwest Computer Club meets at 7:00 p.m., Pacific Science Center, Seattle, WA. General Meeting. Details of agenda: call (206) 524-6359.

Jan. 20 South Florida Computer Group, Ft. Lauderdale Division meets at 7:30 p.m., FPL, 501 S. Andrews, Ft. Lauderdale, FL. Call (305) 522-5358 for more details.

Jan. 22 Minnesota Computer Society, 7:30 p.m., Hennepin County Library, Southdale Branch, 7001 York Ave South, Edina, MN. For meeting agenda write, MCS, P.O. Box 35317, Minneapolis, MN 55435.

Jan. 30 Chicago Area Computer Hobbyists Exchange (CACHE) meets at 12:00 noon, NIGAS Bldg., Schermer Rd., Glenview IL. LSI-11 Conference, Digital Equipment Corporation Show. Call Bill Precht at (312) 620-1671 or P.O. Box 36, Vernon Hills, IL 60061.

Feb. 1 El Paso Computer Group meets at 7:00 p.m. Meeting place by calling (915) 544-1542.

Feb. 2 New England Computer Society, Inc. meets at 7:00 p.m., MITRE Corp., Cafeteria, Route 62, Bedford MA. Call Dave Day for more information at (603) 434-4239.

Feb. 5 Louisville Area Computer Club meets at 1:00 p.m., Speed Auditorium, University of Louisville. General meeting. Contact Glen Darwin (502) 456-5589 or by writing at 3028 Hunsinger Ln., Louisville, KY 40200.

Feb. 7 AMRAD Amateur Radio Research and Development Corp. meets at 8:00 p.m. in the Patrick Henry Library, Vienna, VA 22101. Call (703) 356-8918 for details.

Feb. 11 Crescent City Computer Club meets at 8:00 p.m., University of New Orleans, Lakefront Campus. For more information contact Bob Latham (504) 722-6321.

Feb. 11 Rochester Area Microcomputer Society, 6:30 p.m., Room 1030, Bldg. 9, Rochester Institute of Technology, Rochester, NY. Mailing address, RAMS, P.O. Box D, Rochester, NY 14609.

Feb. 12 The Permian Basin Computer Group, Midland Chapter meets at 4:00 p.m., Midland College, Occupational Technology Bldg., Room 110. General Meeting. Call (915) 697-4607 for details.

Feb. 12 The Permian Basin Computer Group, Odessa Chapter meets at 1:00 p.m., Odessa College Electronics Technology Bldg., Room 203. Call (915) 332-9151 for more information.

Feb. 12 So. Cal. SWTPO MP 6800 Users Group meets at 10:00 a.m. at A-VID Electronics, 1655 E. 28th Street, Long Beach CA 70806.

Feb. 27 Chicago Area Computer Hobbyists Exchange (CACHE) meets at 12:00 noon, NIGAS Bldg., Schermer Rd., Glenview IL. Sick Computer Show. Bring in your problems and we'll help repair them. Call Bill Precht at (312) 620-1671.

Feb. 28-Mar. 3 IEEE Computer Society's COMPCON '77 Spring beginning at 9:00 a.m. on Feb. 28 at the Jack Tar Hotel, San Francisco, California.

Mar. 2 New England Computer Society, Inc., meets at 7:00 p.m., MITRE Corp., Cafeteria, Route 62, Bedford, MA. General Meeting. Call Dave Day at (603) 434-4239.

Mar. 7 AMRAD Amateur Radio Research and Development Corp. meets at 8:00 p.m. in the Patrick Henry Library, Vienna, VA 22101. Call (703) 356-8918 for details.

Mar. 10 Rochester Area Microcomputer Society, 6:30, Room 1030, Bldg. 9, Rochester Institute of Technology, Rochester, NY. Mailing address, RAMS, P.O. Box D, Rochester, NY 14609

Mar. 27 Chicago Area Computer Hobbyists Exchange (CACHE) meets at 12:00 noon, NIGAS Bldg., Schermer Rd., Glenview, IL. Small Business Opportunities Show. For further information contact Bill Precht (312) 620-1671.

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Letters to the Editor

Dear Editor:

I would like to thank you for having taken the time to discuss with me my problem in finding any MIKBUG documentation.

I would like to comment on the above problem. I am an engineer at a small company which provides analysis and programming services as well as designing test apparatus and providing test conductors. This work has been done both for larger companies and directly for government agencies, primarily branches of the Navy. My own areas are dynamics and system modeling. My programming is done in FORTRAN and my method of computer access is thru TSO. I have become aware of the possibilities of the microcomputer and the various available peripherals for my own use in such areas as text editing and for use by our test personnel in various ways. I have accordingly set out to try to educate myself in the ways of the microcomputer both for the good of my company and for selfish reasons. I think that engineers far removed from electronics will need to understand the intelligent machines to continue to be fully useful. At any rate, the point I was going to make is that my personal quest for information will shape the views I pass on to my employer(s), and if I find myself in a position to recommend some device or some supplier, it will be one who has been both willing and capable of supplying me with information, as well as being interested in providing access to their product in small or unit lots. This isn't to suggest that they supply free samples, but rather that they see to it that there are retail dealers who are knowledgeable as to their merchandise and who are responsive to small orders. It is a case of casting their bread upon the water . . . I would suspect that a significant percentage of the people who are interested in microprocessors, etc. as an avocation or for home applications are professionals in fields in which these same devices might find use. Thus, a manufacturer who gives adequate

attention to the personal computing market is probably effectively advertising in the commercial market which he sees as his real target. I would like to suggest that you carry on a dialogue with the major manufacturers along these lines and base an article on it.

Thank you for the interesting and useful magazine which you produce and thank you in advance for the MIKBUG data.

Philip Sollow

Dear Editor:

I presently own two microcomputers, one is a 6800 based system and the other is an 8080 based system, and I am searching for software with which to operate my computers for my business.

I am particularly interested in programs that involve inventory control, payroll, ledgers, journals, balance sheets, income statements, profit and loss statements, invoicing and in general any programs which will perform basic bookkeeping tasks and accounting tasks for a small business.

I would very much appreciate any information that you have concerning software that is business related, as well as any other categories that you might have available (such as games etc.). Such information should include a description of the program, your price, and the length of the program. Any speed and consideration that you could lend to this matter will be greatly appreciated. Thanking you, I remain

James E. Preston

There is a three volume set of books called BASIC Software Library published by R. W. Brown of SRI and available from the Microcomputer Software Depository that includes small business programs — see the Book Review section of this issue for more information.

Software Editor

Dear Editor:

I am a home computer hobbyist presently utilizing a homebrew 8080 system. I have a cassette interface and a TV typewriter. I am looking to expand and/or update my system with the latest hardware developments. Also of interest is software especially BASIC.

Please send me any information you have concerning your software products. Your cooperation is appreciated.

Rupert Fenequito

Dear Editor:

I am enclosing a SASE and a check for \$10, payable to Interface Age, for a one year subscription.

Please send me your list of available software for 8080A based microcomputers. My interests are primarily two fold: (1) Scientific programming (for which I will need FORTRAN or Extended BASIC compilers) and (2) Data Processing for which I could use a good monitor and DOS.

Dennis Eisen

Dear Editor:

I just received my copy of the November issue of INTERFACE AGE and would like to congratulate you on the job you're doing in the Software area. I hope that we can get a Cassette Operating System for the 8080 as a contributed program in the near future.

In your introduction on page 92, you indicated in the second paragraph that an 8080 program by T. W. Travis on memory diagnostics would be published. It appears that it is missing. It is also referenced in the Software Depository Listing on page 128 as appearing in VI NIZ. I trust it will be published in the next issue.

You also indicated that voting for the best article of the month would have to be accomplished by the last date of the month on the issue. As you can see that may eliminate those who receive the magazine late. How about the middle of the following month?

By the way, is there anyone in the SCCS who responds to letters? I know that INTERFACE AGE is not connected with SCCS but from the East Coast it appears that SCCS is dead.

It would be helpful to make a point on the software of indicating how much memory is required for the program and how much memory is required to run the program — when possible — and also if the program can be in PROM or whether RAM is necessary. This would definitely be of help in the Depository listings.

Thanks again for instituting a means of obtaining low cost software.

R. I. Demrow

As you now know we ran out of space for the November issue and had to publish the article Memory Diagnostics by T. W. Travis in the December issue of INTERFACE AGE. We goofed and left all references to this article in the November issue.

Best article of the month voting deadline is the month following date of publication.

INTRODUCING THE WORLD'S FIRST GPGPPDM*

MERLIN

THE INTELLIGENT VIDEO INTERFACE

Is your Altair/IMSAI computer system shy — anemic — withdrawn? Does it just sit there dumbly blinking its pretty lights at you?

Hobbitville's favorite wizard has the best prescription yet for building that full bodied computer system. MERLIN is guaranteed to transform the most introverted blinking light box into an exceptionally communicative extrovert by enabling it to display both ASCII characters (40 columns by 20 lines) and graphics (160H by 100V) on a conventional TV monitor or slightly modified TV. But don't think that MERLIN is all talk and no listen — a parallel input port and plenty of extra power is available to directly tie in most keyboards. An extra serial I/O port may be used for cassette interfaces, joysticks, switches, or properly interfaced smoke signals.

That should be more than enough for a compact, inexpensive two board plug-in system. But not for the wizards at MiniTerm — so there is space for on-board intelligence as well (two 2708 1K X 8 EAROMs or two 2K X 8 ROMs). Yes, as an option MERLIN even comes fully, or partially, educated! The first optional ROM (MBI) includes extensive Monitor/Editor intelligence to help you write, edit, debug, and execute programs. The second optional (MEI) ROM helps you draw pictures and perform cassette I/O (at 1500 BAUD!).

S. An add-on board will be available shortly to expand MERLIN's magical powers into the realm of COLOR and super dense (320H X 200V) graphics!

General Purpose Game Playing Program Development Magician.

WARNING: The Surgeon Jeneral's office has determined that combining blinking light boxes (alias hobbyist Computers) with the MERLIN ASCII/Graphics/Keyboard/Cassette Intelligent Interface is Highly Addicting!!!

PLEASE SEND

- ☐ MERLIN: assembled and tested including manual (does not include memory) \$349.00
- ☐ MERLIN: kit containing PC boards, IC sockets, User Manual and all parts except memory \$249.00
- ☐ MBI, MERLIN'S BASIC INTELLIGENCE: 256 X 8 RAM and 2K X 8 mask ROM containing Monitor/Editor \$ 39.95
- ☐ MEI, MERLIN'S EXPANDED INTELLIGENCE: 2K X 8 mask ROM with more Monitor/Editor functions and Graphics subroutines \$ 34.95
- ☐ MERLIN User Manual: over 100 pages of detailed hardware and software documentation (deductible from kit or assembled MERLIN orders) \$ 8.00

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JANUARY 1977

Box 268, Bedford, Mass. 01730 (617) 648-1200
CIRCLE INQUIRY NO. 18

INTERFACE AGE 15

A CRT Terminal Using the M6800 Family

By Joe Roy and Dusty Morris

Data Processing Systems Engineering
Motorola Inc., Phoenix, AZ

This article describes a versatile M6800 based CRT Controller for "glass-teletype," smart, programmable, and intelligent CRT terminals. While a complete duplication of the entire package may be beyond the capabilities of most readers, some of the design features should be of particular utility in other construction projects. Of particular interest is the exploitation of the bi-phase clock architecture of the M6800 system, providing higher throughput, more I/O handling capability, less interference patterns during refresh memory accesses, and easier task-orientated multiple processor implementation in a CRT terminal than is possible with other approaches. Let's look at the features of this CRT terminal:

1. 24 rows of 80 characters.
2. 7 X 9 uppercase characters in a 9 X 12 dot block; shifted lower case through the use of a custom programmed MCM6832 16K Binary ROM.
3. Conventional non-interlaced raster scan.
4. Blink, half-intensity, video invert, underline, and non-display FACS (Field Attribute Codes); embedded FACS with optional widened memory capability.
5. Alternating inverted/non-inverted cursor.
6. 50/60 Hz field rate is logic selectable; display is centered for both 50 and 60 Hz.
7. Transparent accesses of Refresh Memory by VIA and MPU.
8. Limited graphics implementation with no changes in basic design philosophy.
9. Design philosophy facilitates up-grading a simple economical terminal with upward compatible software and hardware to a task-oriented multiple processor intelligent terminal.
10. MPU is unburdened from overhead of refresh memory contention and is free to service keyboard, edit functions, serial communications, and high speed control such as floppy disk.

The basic configuration for a microprocessor-controlled CRT terminal is shown in Figure 1. An MC6800 microprocessor executes the CRT terminal executive firmware routine and jumps to driver sub-routines when servicing the keyboard, serial synchronous or asynchronous interface, floppy disk formatter, and other peripherals. Cursor movements, R/W, and all editing functions are programmable and under microprocessor control. Actual refresh of the CRT monitor display is done with a configuration of SSI/MSI hardware called a VIA (Video Interface Adapter). The VIA provides video, vertical sync, and horizontal sync to the Motorola M3000 (or equivalent) monitor. The monitor must meet the requirements specified in Figure 2.

The MPU and VIA share the CRT Refresh Memory. Since the processor clock is derived from the VIA, both are synchronized. As shown in Figure 1 timing diagram, the VIA accesses memory for CRT refresh during clock phase $\phi 1$, while the MPU accesses memory during $\phi 2$. The Refresh Memory is organized in an odd address block and an even address block. Both an even and the adjacent odd address characters are transferred during a $\phi 1$ access, whereas a single character is transferred to the MPU during a $\phi 2$ access. The "odd/even memory" concept allows characters to be pulled from memory at a rate (≈ 2 MHz) sufficient to update the CRT. The "interleaved clocking" of memory makes it look transparent to both the MPU and the VIA. That is, neither delays the access of the other to memory. Consequently, less MPU overhead results than in other approaches.

Note that the interleaved clocking of memory is unaffected by cycle stretching of either MPU $\phi 1$ or $\phi 2$... techniques used for refreshing dynamic memories, synchronizing other I/O, or interfacing slow memory.

The Refresh Memory provides a bidirectional data bus to the MPU and a two byte output bus for screen refresh. The two bytes of display data are pipelined to even and odd latches which are alternately enabled as data to the address inputs of an MCM6832 character ROM. The address is an ASCII character which the

- Single M6800 Microprocessor Controls CRT, Keyboard, Serial Communications Interface, and Jolly Disk in Smart/Intelligent CRT terminal.
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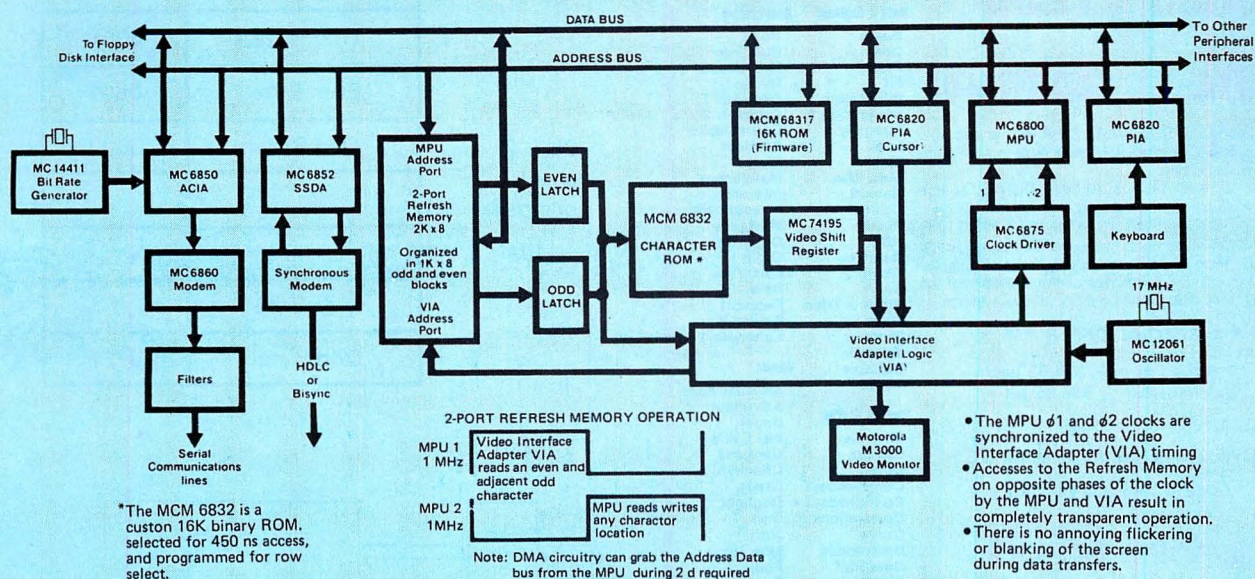


Figure 1. M6800 Terminal Block Diagram

1. Character Matrix	(Columns	7	7
2.	(Rows	9	9
3. Character Block	(Columns	9	9
4.	(Rows	12	12
5. Frame (refresh) Rate		50 HZ	60 HZ
6. Rows of Characters		24	24
7. Active Scan Lines (line 6 times line 4)		288	288
8. Delay before Vertical Sync (No. of scan lines)	4.52 ms	(1667ms) 31	0
9. Vertical Sync Width (No. of scan lines)		(215ms) 4	4 (215ms)
10. Delay after Vertical Sync (No. of scan lines)		(2634ms) 49	18 (968ms)
11. Total Scan Lines (Line 7+8+9+10)		372	310
12. Horizontal Frequency (line rate) (line 11 times line 5)		(53.76ms) 18.6 KHZ	18.6 KHZ (53.76ms)
13. Character Rate (line 12 times line 18)		1.8972 MHZ	1.8972 MHZ
14. Characters/Rows		80	80
15. Delay before Horiz. Sync, usec: (Character times)		(2.1ms) 4	4 (2.1ms)
16. Horizontal Sync Width usec: (Character times)		(4.7ms) 9	9 (4.7ms)
17. Delay after Horiz. Sync, usec: (Character times)		(4.7ms) 9	9 (4.7ms)
18. Total character times (line 14+15+16+17)		102 (11.5ms)	102 (11.5ms)
19. Clock Rate (line 13 times line 3)		17.074800 MHZ	17.074800 MHZ
20. Display size		12"	12"
21. Character Time (reciprocal of line 13)		527 ms	527 ms
22. MPU Clock (line 19÷2X line 3)		948.6 KHZ	948.6 KHZ
23. Clock Time (reciprocal of line 19)		58.6 ms	58.6 ms

Figure 2 Video Monitor Timing
(Motorola Display Products M3000
Monitor meets these requirements)

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Polynomial
Regression
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T-Distribution
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Variance 2
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Building
Compound
Cyclic
Decision 1
Decision 2
Depreciation
Efficient
Flow
Installment
Interest
Investments
Mortgage
Optimize
Order
Part Tree
Rate
Return 1
Return 2
Schedule 1

Games

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Astronaut
Bagel
Bio Cycle
Cannons
Checkers
Craps
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Golf
Judy
Line Up
Pony
Roulette
Sky Diver
Tank
Teach Me

Pictures

A. Newman
J.F.K.
Linus
Ms. Santa
Nixon
Noel Noel
Nude
Peace

Hex Address

Even Byte	0000
Odd Byte	0001
Even Byte	0002
Odd Byte	0003
...	
Even Byte	
Odd Byte	07FF

2K x 8
equals
one page

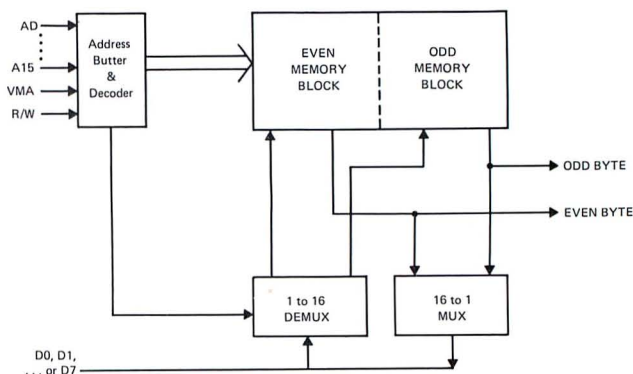


Figure 3.

CIRCLE INQUIRY NO. 28

ROM maps into a block of dots. The particular row of dots (0 to 11) in the block is determined by four "row select" inputs from the VIA. In a raster scan system, each ASCII character is presented 12 times to the character ROM with a sequential row select each time in order to paint the complete character on the screen.

Each row of dots is parallel loaded into an 8 bit shift register and clocked out serially. Field Attribute Codes (FACS) such as inverted video are imposed on the serial data stream by the VIA before the video is sent to the monitor.

This section describes the 2 port memory technique which allows interleaving of the MPU and display functions with minimal interference. Figure 3 is a simplified block diagram of the functional implementation. As can be seen the memory is divided into two blocks; one 'even' and one 'odd.' Selection of the appropriate block is by address line AO, while A1 through A10 select one of the 1024 bytes in each block. A11 through A13 are used to select the particular "page" of memory. R/W and VMA are used in the read/write process and to determine if data is gated 'in' or 'out' on the data line D0 through D7.

As described earlier, the refresh RAM is organized as a 1K X 8 even block and a 1K X 8 odd block.

Even and odd blocks are interleaved to form a 2K X 8 "page." Of the 2048 bytes, 1920 (80 times 24) are required per page of display, leaving 128 bytes spare. Because the refresh memory looks like any other RAM on the MPU bus, this spare 128 bytes are free for scratch and the stack. In multiple page systems, it serves as an edit buffer.

The refresh memory is implemented with 450ns 2102 style 1K X 1 memories. Even and odd blocks each contain eight devices. The new 2114 style 1K X 4 static memories (spec'd at 450ns) are an attractive alternate (only four are required per page). Memory addressing is through 1 of 2 ports. Referring to Figure 4, the schematic offers the two port memory, we will look into the detailed design.

The VIA address counter (DA1-DA10) is gated with a set of MC6887 high speed three state buffers, the Motorola equivalent of the 8797 device. The enable signal to pins 1 and 15 on U20 and U21 is generated only during EN DISP ADDR at P2 pin 3 (roughly 01 interval) and when PAGE SELECT is high at P2 pin 4. The latter signal is only required in multiple page systems, and determined which page is displayed. Note that pin 15 on U20 is always enabled. This gates pin 12 to 11 path buffers VMA (Valid Memory Address). This signal is for gating the MPU address buffers (U18 and U19). When used with systems such as the EXOR-cisor where a block of addresses must be unconditionally protected, this signal should be VUA (Valid Users Address).



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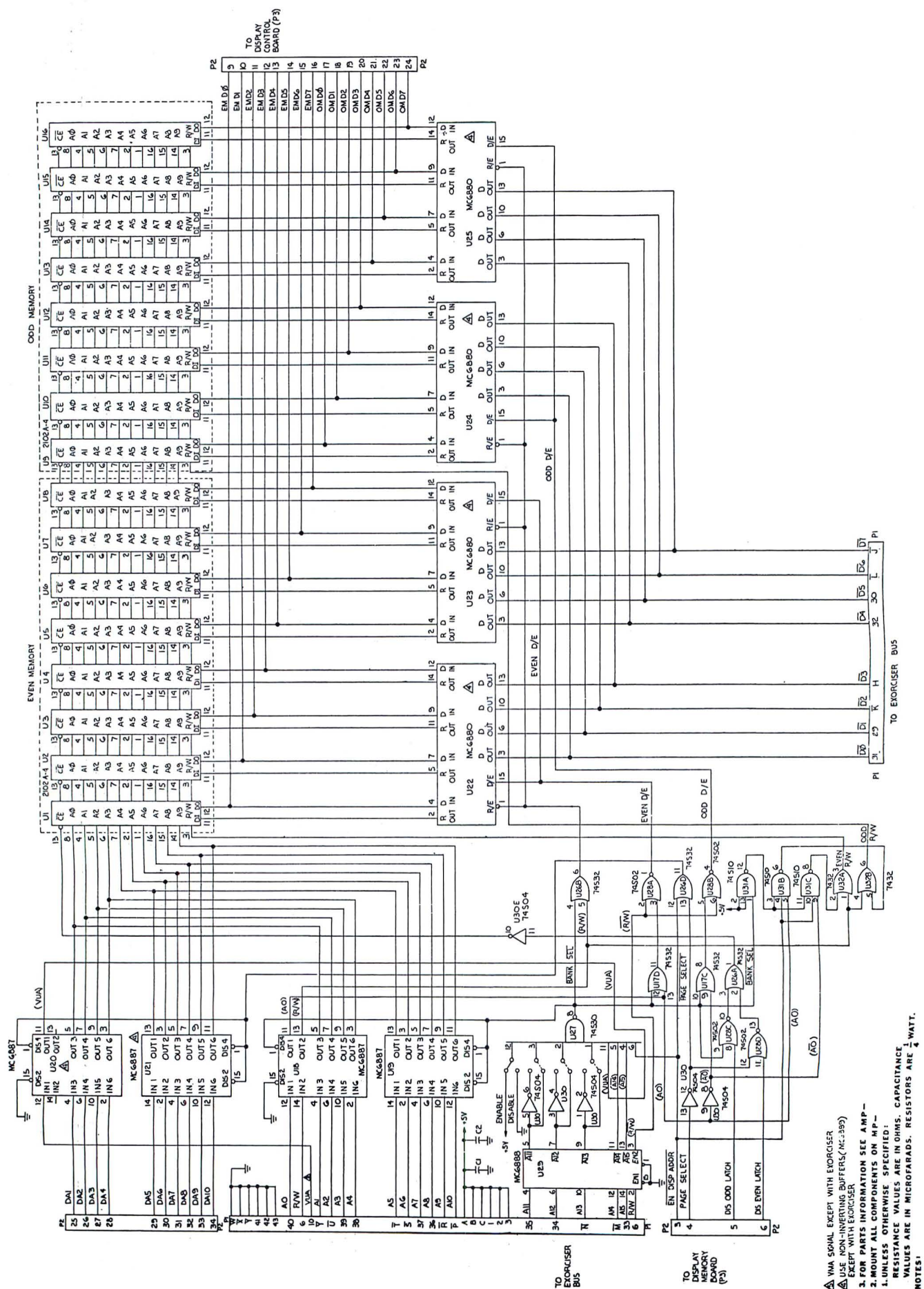


Figure 4. Display Memory Board



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The selection of U18 and U19 is decoded by U27 which generates BANK Select. The particular bank (1 of 8 pages) is strap selectable (U29 and U30). The ENABLE/DISABLE switch on U27 provides a means of overlaying other chunks of memory with the same address. The other gating for BANK SELECT is VMA (described above), A14, A15, and EN DISP ADDR (EN MPU or roughly $\emptyset 2$ interval). AO and R/W from the MPU are gated at all times because pin 15 on U18 is tied to ground.

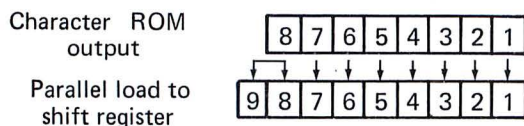
Devices U22 through U25 are MC6880 high speed bidirectional data buffers for multiplexing the Even and Odd Memory bytes into the MPU data bus ($\overline{DO} - \overline{D7}$) and vice versa. In systems requiring a non-inverted data bus, MC6880 is replaced with MC6889. During an MPU read, either U22/U23 or U24/U25 is enabled by EVEN D/E or ODD D/E respectively. The buffered LSB of the MPU address, AO, determines which signal is active. During an MPU write, both U22/U23 and U24/U25 are enabled into their respective Even and Odd Memory blocks. The buffered LSB of the MPU address, AO, determines whether EVEN R/W or ODD R/W is active.

The refresh data is an even byte (EMD \emptyset -7) and an odd byte (OMD \emptyset -7).

Memory for Graphics Applications

Alphanumeric refresh memories are organized on a character basis. Each code stored in memory represents a 7 X 9 pattern in a 9 X 12 dot block. The dot pattern is stored in a character ROM addressed by the character code in the RAM. The repetition of a limited set of symbols on the screen to construct messages makes it possible to use a smaller amount of memory than would be required in a full graphics application where every dot is addressable as a memory location.

A "limited" graphics set of symbols for line drawings and forms is usually implemented with a special character ROM. The nine horizontal dots per character are provided by the ROM. However, most ROMs are organized by eight. It is usually acceptable to get the ninth bit from one of the eight ROM outputs, by parallel load of the 8th bit of ROM into both the eighth and ninth bits of the shift register.



A full graphics capability requires every possible dot on the screen to be stored in memory. Since the pattern is stored directly in RAM, all alphanumeric patterns are generated external to the refresh loop. Accordingly, the character ROM is placed on the MPU bus, and the dual latches drive the shift register directly. As in the alphanumeric controller, the RAM delivers two bytes (even and odd) when addressed by the VIA for refresh. Read and write addressing by the MPU is efficiently handled by bit addressing rather than byte addressing. The complete 64 K address structure of the MC6800 is decoded by hardware; only one of the eight MPU data bits is used for transfers.

A graphics terminal dedicates an MPU to the keyboard and I/O transfers with the refresh memory. All calculations (e.g. vectors), curves, rotations are done in an outboard high speed processor (e.g. microprogrammed bipolar slice). An interface between the MPU and the higher speed processor provides means for control and exchange of input parameters and results.

DISPLAY CONTROL

The DISPLAY CONTROL consists of circuitry to: sequentially access ASCII characters from the 2-PORT REFRESH MEMORY; generate character row selects; load row patterns into the Parallel-to-Serial Shift Register; serially shift the row pattern through Field Attribute circuits to the monitor as video; provide blanking, horizontal sync, and vertical sync signals; perform cursor compare and generate cursor block.

Character ROM

The purpose of the Display Control circuitry is to paint the contents of the character ROM at the designated positions on the CRT screen. Custom character ROMs contain 9 X 16 dot matrix patterns for alpha-numeric characters of various domestic and foreign fonts, limited graphics symbols, control characters, or combinations of all from the above. The addresses of the character dot matrix patterns correspond to their ASCII code representation in the case of alphanumeric and control characters. (Assignment is somewhat arbitrary for graphic symbols.)

The particular row of dots in each character dot matrix is selected by four binary row select inputs. Only 12 of the possible 16 rows are utilized in the CRT display being described. The 12 rows are adequate for shifted lower-case characters (g, j, p, q).

Referring to Figure 5 we see that a 16 K binary ROM (e.g. MCM6832) provides 128 possible ASCII characters (only 7 X 12 of the 8 X 16 dot block is used). This is a practical number of characters for most applications. Note the eighth bit of the ASCII code is always available. If it is not used for imbedded Field Attribute Codes (see FAC circuitry description), it can be used to select a second MCM6832 with a different font or graphics. The tri-state capability of the MCM6832 facilitates this mode of operation.

General Timing

All timing, including MPU $\emptyset 1$ and $\emptyset 2$ is derived from an MC12061 crystal oscillator running at the video rate, 17.074800 MHz. The circuit is very stable and always starts from power up. The TTL output of the MC12061 is buffered with a 74S04 before distributing the clock to avoid distortion. The distribution of the clock is critical. Video Clock and Video Clock are fanned out using 74S04 inverters in the same package (for minimum differential propagation delay). Loads are split equally. An alternate distributor is a high speed clock driver with complementary outputs. An important consideration is to keep all 17 MHz logic close together and in proximity to a ground. This will minimize noise and distortion.

There is another method for arriving at 17.074800 MHz. Although it is more expensive, a phase-locked

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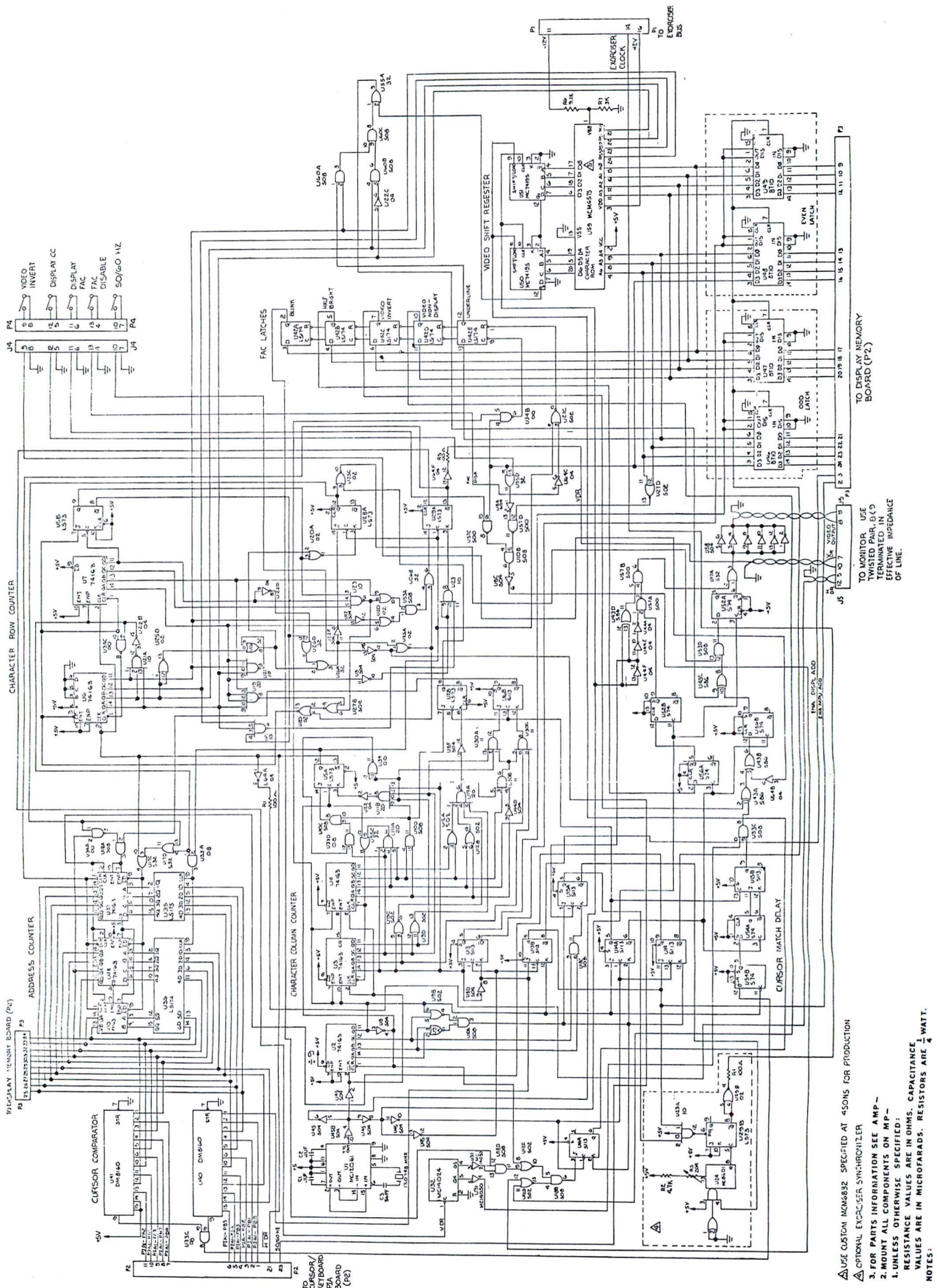
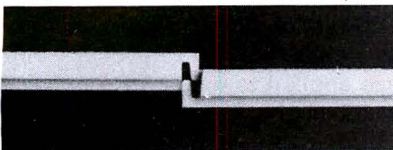


Figure 5. Schematic — Display Control Board

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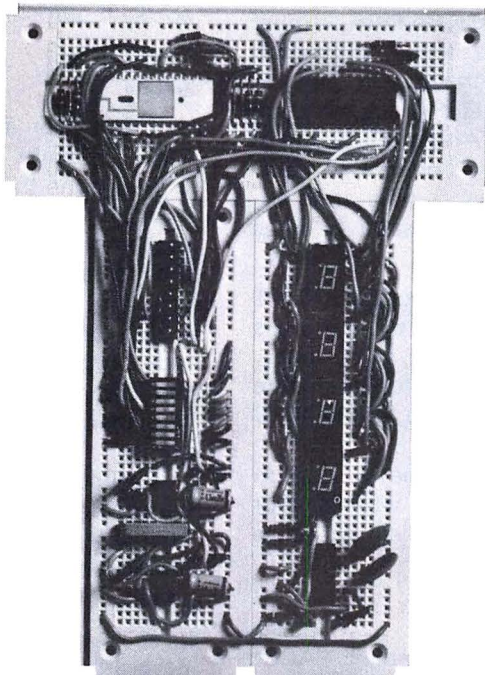
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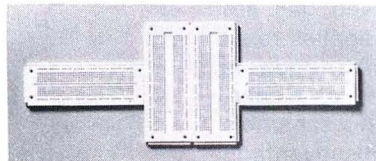
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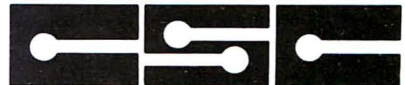


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loop or phase-locked oscillator is used. The line frequency is the reference and vertical sync the comparison signal. In areas where the line frequency varies radically from nominal, the more expensive system is often required to reduce the visible beat on the CRT screen.

A $\div 9$ counter divides video rate down to a character rate of 1.9 MHz. On/Off decodes from the $\div 9$ counter are resynchronized in 74S113 high speed flip flops. The signals provide the General Timing in Figure 6.

Decodes off the Character Column Counter provide horizontal timing (Figure 7). Vertical timing is from the Character Row Counter (Figure 8).

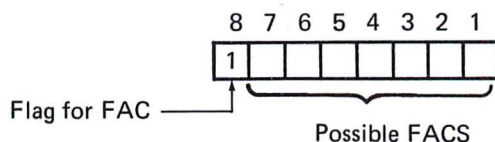
Note the operation of the Address Counter. It must repeat each character address 12 times to paint a complete line of 80 characters on the screen. This requires storing the address of the first character in each line (function of the 74LS latches). Another function of the Address Counter is to advance to address 64 during V blank. (Effectively, this amounts to a start address of 128 since the memory is addressed two bytes at a time.)

Another function of the Display Control Electronics is cursor compare. The contents of the Address Counter are compared with PIA data for coincidence. The DM8160's are exclusive-or comparators. PIA data is a binary address which is manipulated by the MPU for cursor control.

The other circuitry in the Display Control portion generates invert/non-invert cursor block when cursor compare is sensed and furnishes FAC (Field Attribute Code) logic.

FACS (Field Attribute Codes)

There are two popular methods for handling FACS. In the wide memory method, the memory size is increased by adding bits to each character in memory. Each bit controls a different attribute code for that character. The other method imbeds FAC characters in refresh memory. The eighth bit of the ASCII code is usually decoded as a FAC flag.



When it is a logical one, the other seven bits are latched as FACS. Once latched, the FAC applies to all subsequent characters until another FAC code is decoded. The only exception is at the end of a character line; all FACS are hardware reset. This scheme's advantage is low cost to implement; the disadvantage is the use of a memory location per FAC code. Not only is character density decreased, but the individual characters in a string can not be accented with FACS. It is possible to get around this drawback by stripping FACS from the memory before display, but requires extra hardware and is a programming nightmare. When individually accented characters are required, it is usually better to implement a wider memory.

The wide memory approach to FACS may seem clumsy at first glance... the MPU has an 8 bit bus. How are 8 bit MPU transfers done? Construct two pages of memory — a page of ASCII characters 2K X 8, and a page of attributes (2K X 1, 2, 3, 4, ..., 8). The attribute page is a mask and need only be accessed when the attribute changes or must be read.

For simplicity, the imbedded FAC method was implemented in the CRT terminal. Few changes in Display Control circuitry are required for a wide memory approach.

CURSOR/KEYBOARD

Referring to Figure 9 we can see how to add a cursor/keyboard interface to this "glass teletype."

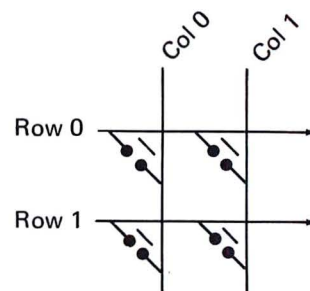
Cursor

The cursor address is stored as the contents of a PIA. The eight least significant binary bits are PBO - PB7 and the three most significant binary bits are PA0 - PA2. There is a one-to-one correspondence between the binary cursor address and a memory location on the screen. The assignment of bits in the PIA is for programming convenience. An STX instruction to the A side of the PIA writes the higher order byte of the index register into the A side of the cursor PIA and the lower order byte into the B side of the cursor PIA (provided the address lines to RSO and RS1 are reversed).

The cursor address is binary rather than X-Y because the binary address manipulations are more frequent. When X-Y addressing is required (e.g. communication interface), a conversion subroutine is called.

Keyboard

Either a fully-encoded or non-encoded keyboard can be designed. Whichever, a PIA provides the interface to the MPU. In a fully-encoded keyboard, the keyboard hardware generates a strobe and an ASCII encoded character corresponding to the depressed key. All debounce is handled by the keyboard hardware. The strobe pulse applied to the PIA CA or CB inputs causes an interrupt to the MPU. The MPU reads the ASCII character through the PIA and performs the appropriate function. For an alphanumeric character, the MPU writes the data at the present cursor location and increments cursor PIA contents. For control characters, the corresponding commands are executed. (e.g. space, carriage return, insert, delete, etc.)



A non-encoded keyboard is a set of switches wired in a column/row matrix.

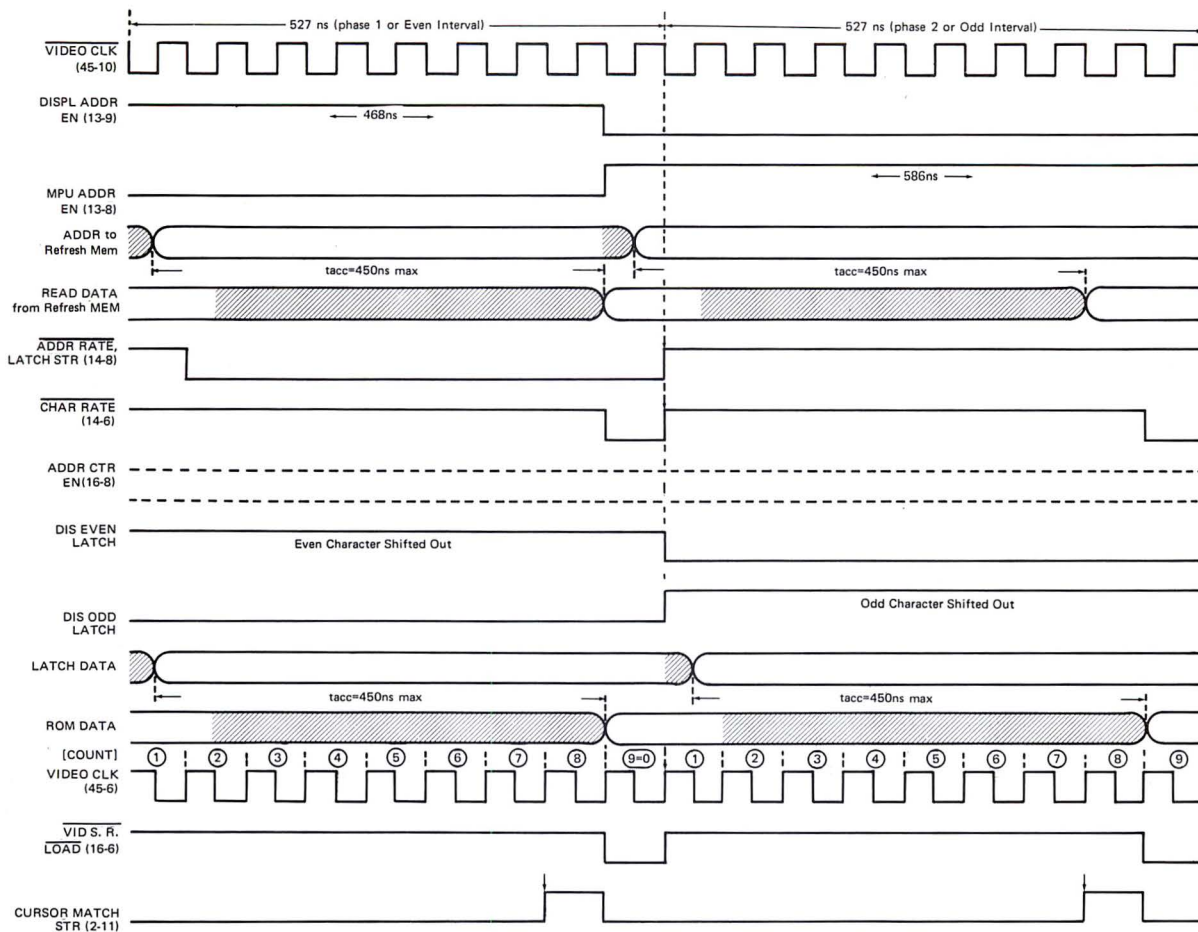


Figure 6. General Timing

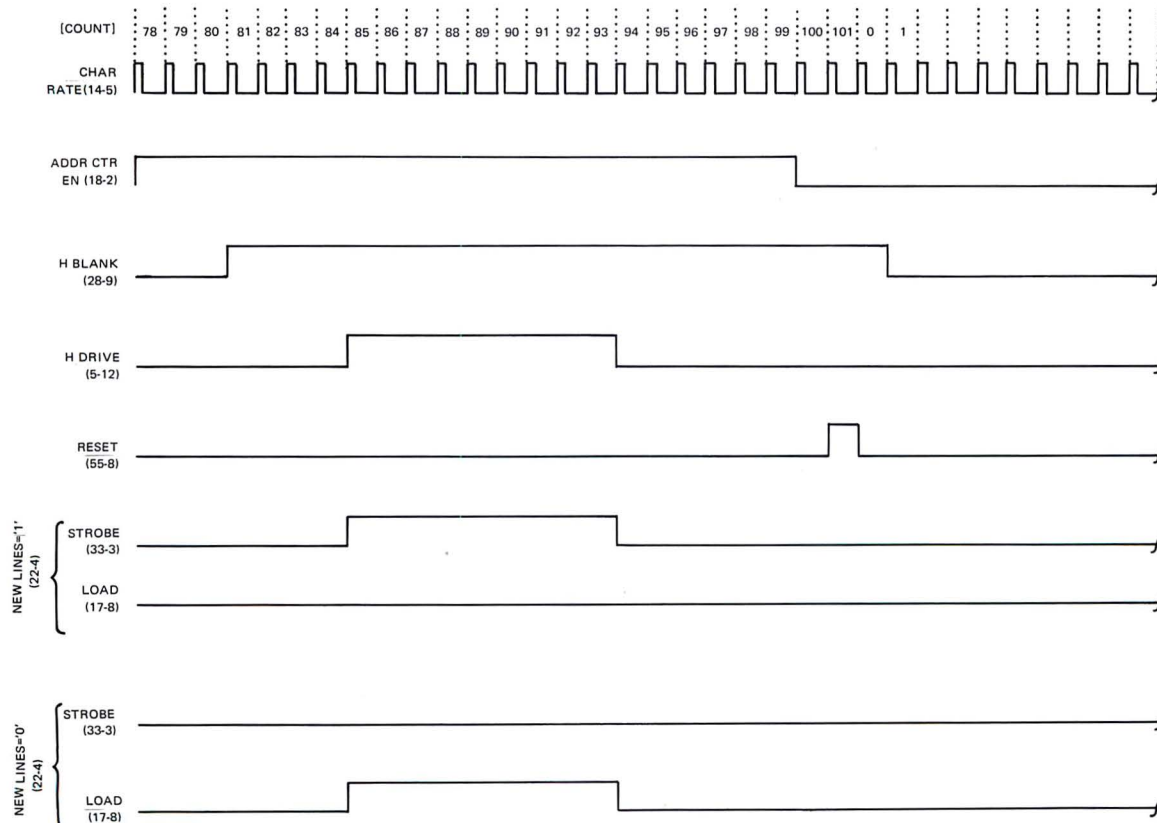


Figure 7. Horizontal Timing

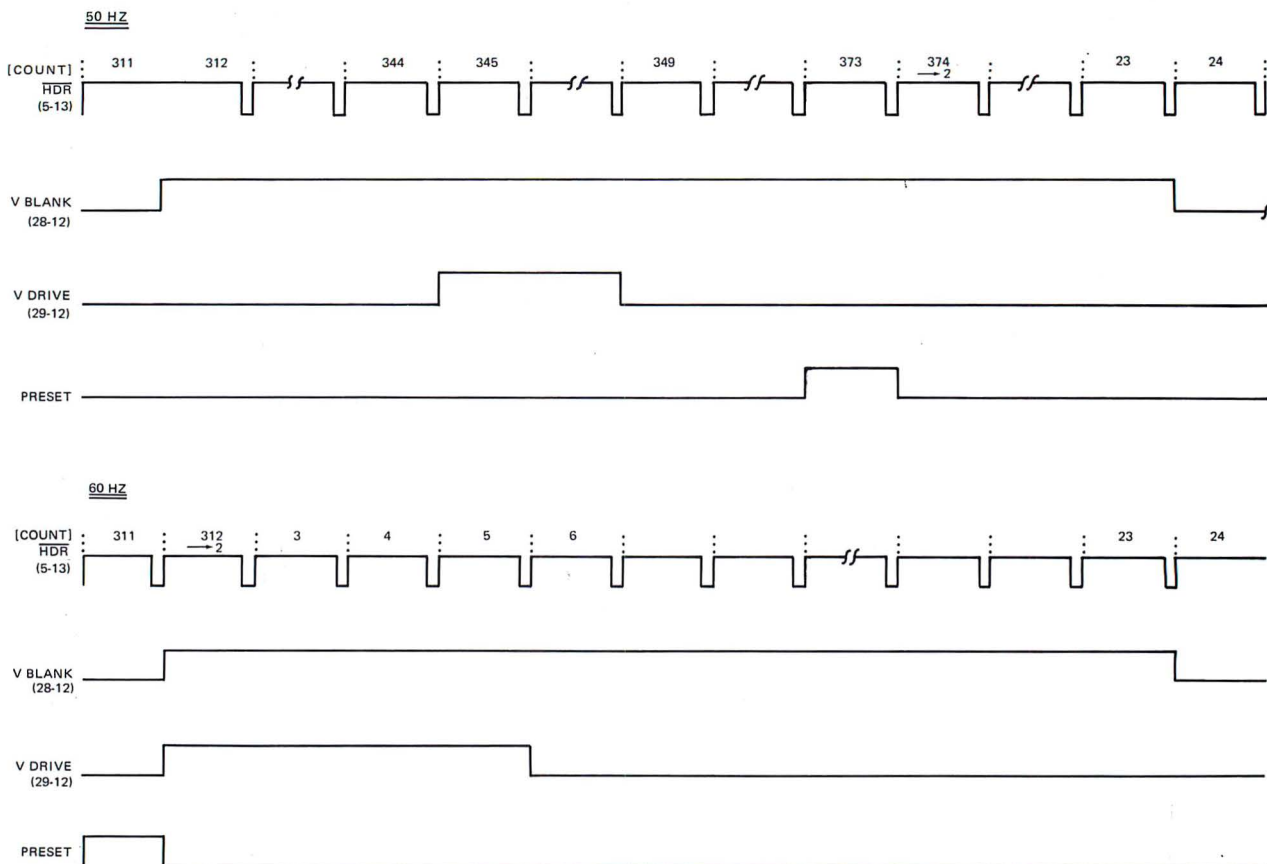
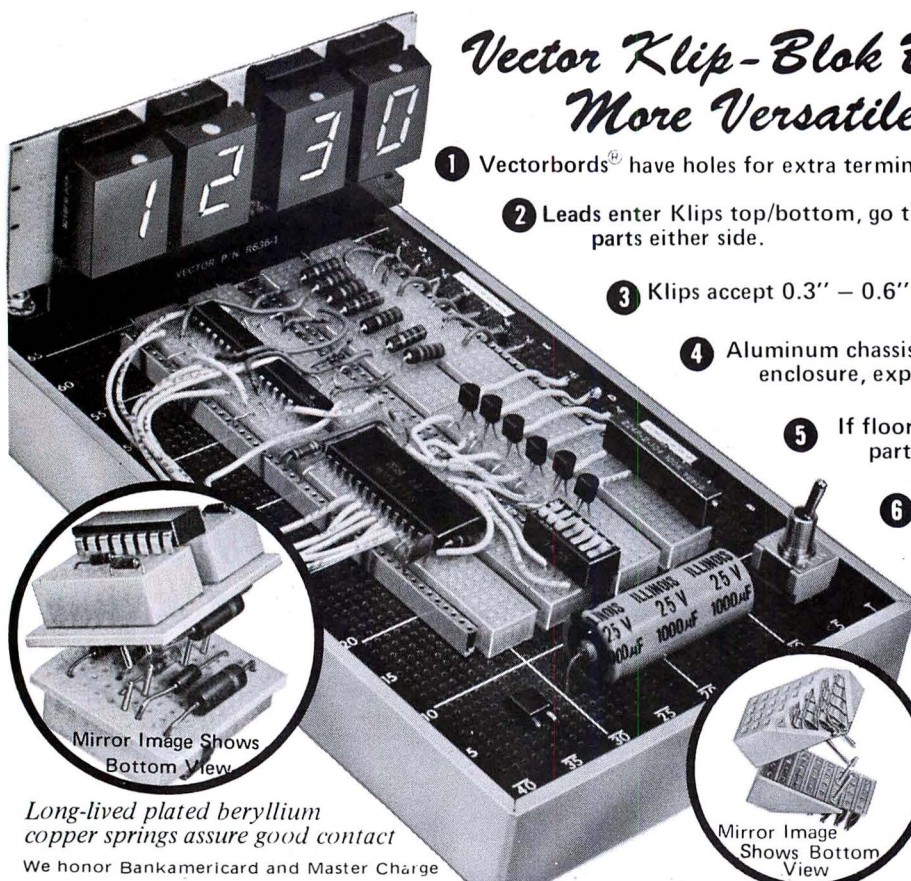


Figure 8. Vertical Timing



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If the columns are scanned one at a time, and the rows read back, the simultaneous depression of any one or two keys can be discerned. For n keys, diodes are wired in series with the switch contacts.

The scanning of columns, reading of rows, and switch debounce are under software control. Keys are strategically placed in the matrix so the column and row location easily translate into an ASCII code. Cost savings and flexibility of this non-encoded keyboard versus a fully-encoded keyboard sometimes justifies the additional MPU overhead in a basic CRT terminal.

A non-encoded approach is described here. Referring to the schematic, the keyboard columns are normally held low. When key(s) are depressed, lows appear on the keyboard row inputs. A keyboard interrupt is generated, which starts a scan. Keyboard column outputs are brought low in sequential order. Together with the Shift and Control PIA inputs, the active columns and rows are encoded as an ASCII character and temporarily stored. A 6.88 msec interrupt is provided for debounce and a PIA input for REPEAT (also .1 sec interrupt for this function and a 1 second interrupt for clock functions).

The software for a non-encoded keyboard ranges from simple to quite complex depending on how fool-proof the algorithm is.

Comparison of CRT Terminal Architectures

The central design criteria of a modern CRT terminal is the method used for multiplexing refresh memory between the MPU and the display refresh circuitry. In this section we will discuss time-division multiplexing and priority multiplexing. Throughput versus hardware complexity for different techniques will be analyzed. Those systems which result in operator annoyance in many applications (e.g. Key-to-Disk), and are not appropriate for the modern CRT terminal.

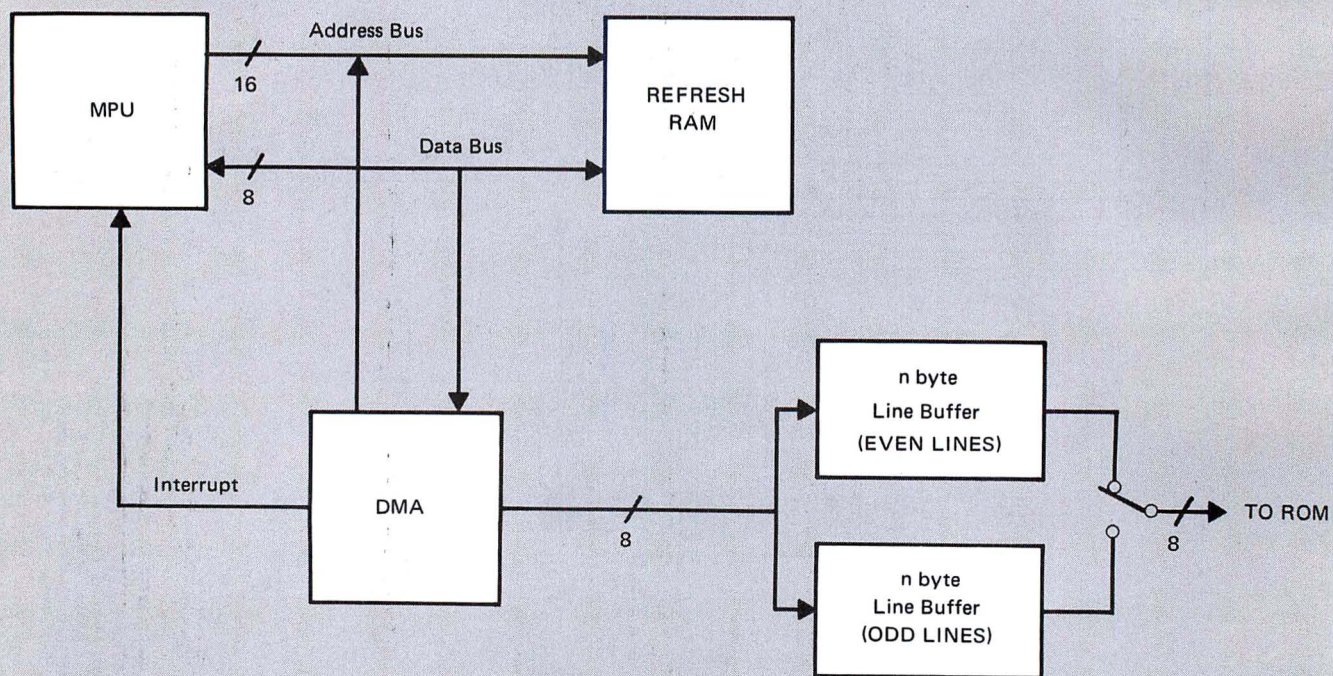
Priority Multiplexing of Refresh Memory

These techniques fall into two general categories:

- A. MPU grabs Refresh Memory and locks out Refresh Circuitry.
- B. Refresh circuitry grabs Refresh Memory and locks out MPU.

Method A results in zero burden on the MPU; however, a sufficient number of refresh characters must be pipe-lined into FIFO to keep the screen refreshed during an MPU access. The fast memory and complex hardware to accomplish this task is unattractive.

Method B is probably the most widespread technique in use today. The dual line buffer approach is



Dual Line Buffering Technique

DIGITAL DATA RECORDERS

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MODEL 3M3
199⁹⁵

MODEL 3M3—Uses the 3M Data Cartridge, Model DC300. This cartridge contains 300 feet of .250 tape in a sealed container. Records and plays at 9600 baud NRZ, 4800 baud P.E. Nominal speed 8" per second. Max. recommended flux density 1200 fcpi. Using four tracks, you can store nearly 2 megabytes of data on a cartridge. Cartridge measures 4" by 6". Turns counter indicates tape position. Inter-record gap light gives more accurate position 2SIO(R) is *not* required for use, but is highly recommended for 8080 and Z80 systems.

COMMON SPECIFICATIONS: FULL SOFTWARE CONTROL of record, play, fast forward and rewind. LED indicates inter-record gaps. EOT and BOT are sensed and automatically shut down recorder. Can also be manually operated using the switches on top which parallel the software control signals when not under software control. Signal feedback makes it possible to software search for inter-record gaps at high speed. 117 V—50 Hz—5 watts.

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\$189.95 (Full Program)

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*Appearance and specifications may be changed slightly following acceptance tests now being conducted by OEM users.

MODEL 3M1—Uses the 3M Data Cartridge type DC100A. This cartridge contains 150 feet of .150 tape and is the same cartridge used by H.P. and others. Runs at 4800 baud NRZ, 2400 baud P.E. Tape speed adjustable, but nominally set at 5"/second. Maximum recommended flux density 1200 fcpi. Cartridge measures 2-1/8" by 3-1/4". This model is ultra compact, yet extremely capable. It is intended for word processing, mailing list use and other applications requiring the compact storage of data. Data location is by inter-record gaps and automatic file search. See Common Specs and 2SIO(R). 2SIO(R) is *not* required for use, but is highly recommended for 8080 and Z80 users.

For 8080 and Z80 users: Comes complete with software program listings for the programs on the 2SIO(R) ROM. 6800 software is being written, but not yet completed. These programs give **FULL SOFTWARE CONTROL.**

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NEW: AUDIO CASSETTE INTERFACE* Phase Encoding interface for use with audio cassettes or NRZ recorders. Runs 2400 baud phase encoded on good quality audio cassette recorders. May also be used with 2SIO(R) to use the 2SIO(R) cassette programs with your audio cassette player. Can also accommodate "Tarbell" tapes and K.C. Std. tapes. \$50.00, Wired & Tested. \$35.00, Kit Form.

***NOTE:** You do not require an interface with the 3M1 and 3M3 unless you Phase Encode. But, you do need an interface to use the 2SIO(R) with your own audio cassette.

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representative of this class. All data for a line on the screen is stored in FIFO's (usually 80 bytes).

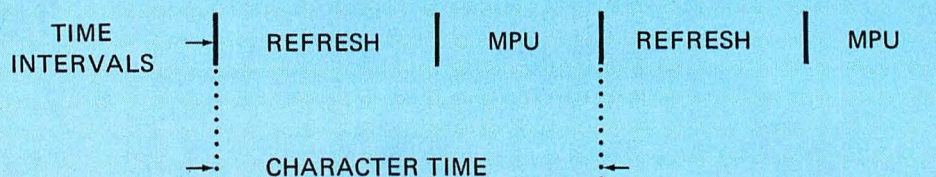
While the Odd line buffer is keeping the display refreshed, the Even line buffer is being filled with the next displayed line from Refresh RAM through a DMA channel. The functions are alternately reversed. In an alphanumeric terminal, average MPU burden is between 15 and 30% with peak burden on the MPU of 100% for 80-100 microseconds when loading either line buffer. The MPU is stalled during this transfer and cannot service high speed interfaces (e.g. Floppy Disk). With the addition of extra hardware, the Refresh page of the RAM is isolated from the processor bus during DMA, thus allowing the MPU to continue processing provided it attempts no accesses to memory. In conclusion, the dual-line buffers and DMA configuration is more expensive, has higher parts count, and imposes a severe burden on the MPU compared to the time-division multiplexed technique.

Furthermore, the DMA approach is very inefficient for full graphics, since there are no recirculations of the line buffer as in an alphanumeric display.

refreshed during an MPU synchronization delay. The FIFO is typically two bytes deep. The disadvantage of this technique is the requirement for fast memory. It is considerably simplified if the time-division multiplexing is made synchronous with character rate. Sync delay is no longer required for refresh and the FIFO circuitry is eliminated (a single byte latch is still required). Also memory speed is reduced. This simplification is not always acceptable; e.g. it may result in excessive MPU "cycle-stretching" at slow character rates.

The technique for sharing CRT Refresh Memory described in this article is a special case of time-division multiplexing. The access intervals for Refresh and MPU are 01 and 02, respectively.

As 01 and 02 clocking signals are outputted even during wait states, no matter how long this MPU is forced into a wait state the screen will remain refreshed. Since there is no overlap of accesses, no contention circuitry is required and the MPU burden is zero at all times. While you may not want or need to duplicate the entire circuitry described in this article, the bi-phase memory access technique may be used

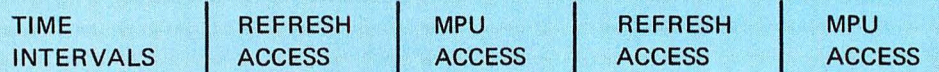


Time Division Multiplexing of Refresh Memory

In the most general time-division multiplexing situation, either an MPU or Refresh access may commence or end asynchronously to time-division multiplexing intervals. By delaying accesses, the MPU and Refresh circuitry are brought in sync with their respective time intervals. The sync delay for MPU access, at the expense of throughput, is implemented by "cycle-stretching." The sync delay for Refresh access is accomplished by pipe lining a sufficient number of refresh characters into a FIFO to keep the screen

wherever it is necessary to use a DMA (Direct Memory Access) for two major systems.

The M6800 implementation is very simple due to constant cycle lengths, whereas it is difficult if not impossible with variable cycle length MPU's. The only drawback to this scheme is that the MPU rate is a derivative of the character rate. This translates into a clock rate lower than the maximum MPU clock rate allowable. Consequently, the throughput is reduced. For example, the screen density in this article reduces the throughput by 5% because the MPU runs at 950 KHz.



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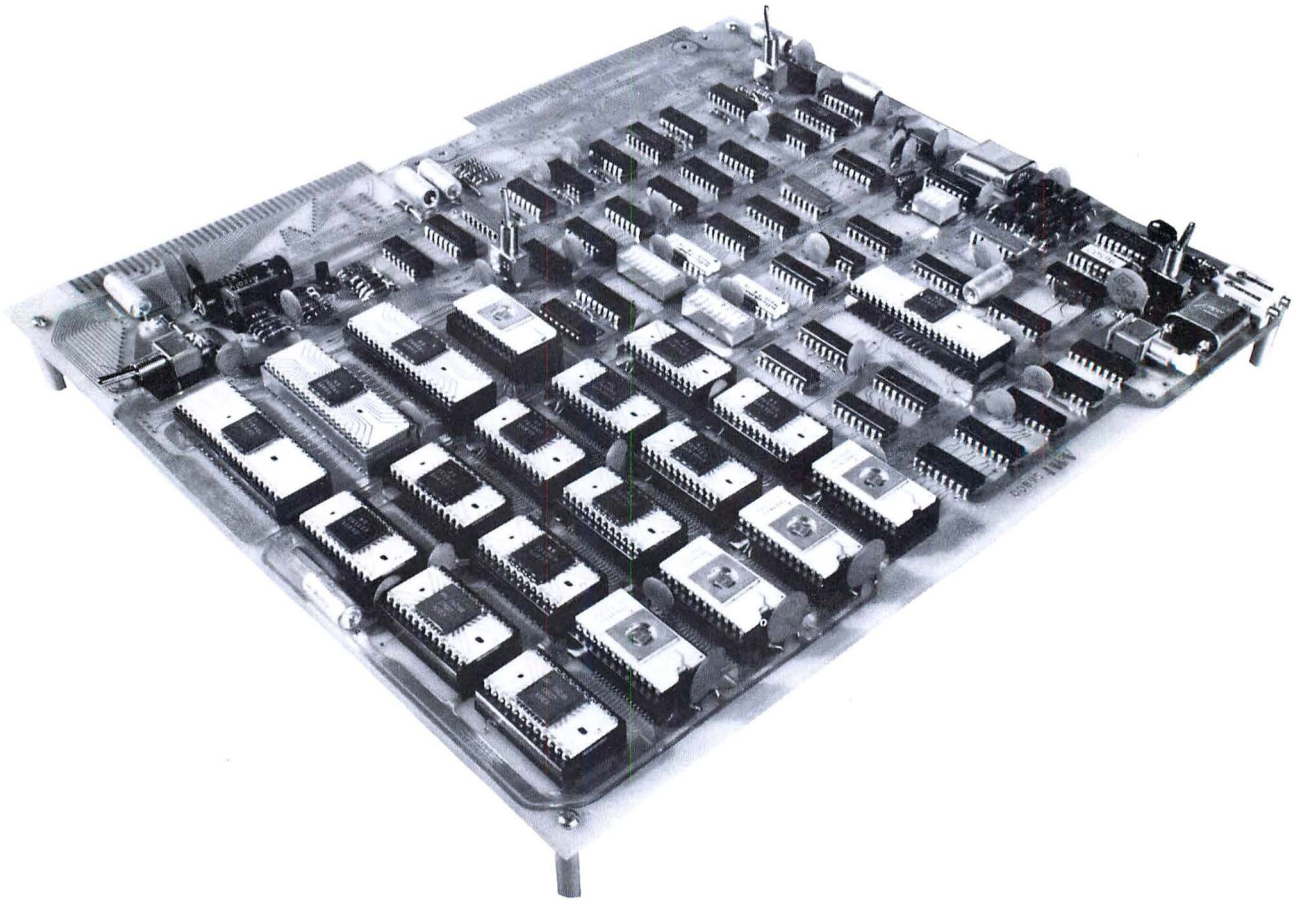
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AMI's EVK Series Microcomputer Prototyping Boards



By Robert A. Stevens

INTRODUCTION

This article is part #2 of a series of articles on the EVK Microcomputer hardware, firmware and supporting software. This month's article covers the EVK Microcomputer board architecture while last month's article described the functional architecture and characteristics of AMI's Microcomputer IC chip set.

EVK CONFIGURATIONS — The AMI EVK Microcomputer is a single board microcomputer mechanized with a standard S6800 MPU. The EVK Microcomputer comes in four basic configurations; EVK99, EVK100, EVK200, & EVK300, all of which use

the same 10½" x 12" printed circuit board. EVK99 is a kit that includes the PCB and Microcomputer ICs consisting of one 6800 MPU, four 6810 RAM's, one 6820 PIA, two 6830 ROM, and one 6850 ACIA. EVK100 & EVK200 are kit configurations that include PCB, Microcomputer & T²L IC's and differ from each other by the amount of hardware, memory and firmware (software in ROM) included with each configuration. EVK300 is the EVK200 kit with more EPROM memory and is factory assembled and tested. A Tiny BASIC Interpreter program is also available at no charge for the EVK300 Microcomputer board. Table 1, EVK Microcomputer Configuration Summary, shows the comparison between the different EVK configurations.

EVK BOARD CHARACTERISTICS	EVK 99	EVK 100	EVK200	EVK300
CPU	S6800	S6800	S6800	S6800
WORD SIZE	8 BITS	8 BITS	8 BITS	8 BITS
ADDRESS BUS	16 BITS (64K)	16 BITS (64K)	16 BITS (64K)	16 BITS (64K)
ROM	2K BYTES S6831 ROM	2K BYTES S6831 ROM	2K BYTES S6831 ROM	2K BYTES S6831 ROM
EPROM — VIRGIN	_____	_____	512 BYTES S6834 EPROM	2K BYTES S6834 EPROM
STATIC RAM	512 BYTES S6810 RAM	512 BYTES S6810 RAM	1K BYTES S6810 RAM	1K BYTES S6810 RAM
EPROM PROGRAMMING	_____	_____	PROGRAMS S6834 EPROM's	PROGRAMS S6834 EPROM's
I/O PORTS	1 PIA=2 PORTS — 8 BITS/PORT	_____	3 PIA's=6 PORTS 8 BITS/PORT	3 PIA's=6 PORTS 8 BITS/PORT
ASR 33/35 TTY SERIAL INTERFACE	ACIA S6850	ACIA S6850 WITH 20ma CURRENT LOOP	ACIA S6850 WITH 20ma CURRENT LOOP	ACIA S6850 WITH 20ma CURRENT LOOP
RS232C EIA SERIAL INTERFACE	ACIA S6850	ACIA S6800	ACIA S6850 WITH EIA RS232C	ACIA S6850 WITH EIA RS232C
INTERVAL TIMER (CRYSTAL)	_____	_____	1 ms & 100 μs TIME INTERVALS	1 ms & 100 μs TIME INTERVALS
MPU CRYSTAL CLOCK	_____	_____	INCLUDED	INCLUDED
CLOCK OUTPUTS (CRYSTAL)	_____	16X BAUD RATE	2.4576 MHz, 1 MHz & 16X BAUD RATE	2.4576 MHz, 1 MHz & 16X BAUD RATE
DMA MODES	_____	_____	HALT MPU MODE, CYCLE STEAL MODE & MUX MODE	HALT MPU MODE, CYCLE STEAL MODE & MUX MODE
RESTART ADDRESS SELECTION	_____	TWO 8 BIT DIP TOGGLE SWITCHES	TWO 8 BIT DIP TOGGLE SWITCHES	TWO 8 BIT DIP TOGGLE SWITCHES
TTY MONITOR SOFTWARE	PROTO ROM RESIDENT	PROTO ROM RESIDENT	PROTO ROM RESIDENT	PROTO ROM RESIDENT
SUBROUTINE PROGRAM LIBRARY SOFTWARE	RS ³ ROM RESIDENT	RS ³ ROM RESIDENT	RS ³ ROM RESIDENT	RS ³ ROM RESIDENT
ROM RESIDENT ASSEMBLER	\$35 ⁰⁰ OPTION	\$35 ⁰⁰ OPTION	\$35 ⁰⁰ OPTION	\$35 ⁰⁰ OPTION
OEM SINGLE QUANTITY PRICE	\$133 ⁰⁰	\$295 ⁰⁰	\$495 ⁰⁰	\$765 ⁰⁰

TABLE 1 EVK MICROCOMPUTER CONFIGURATION SUMMARY

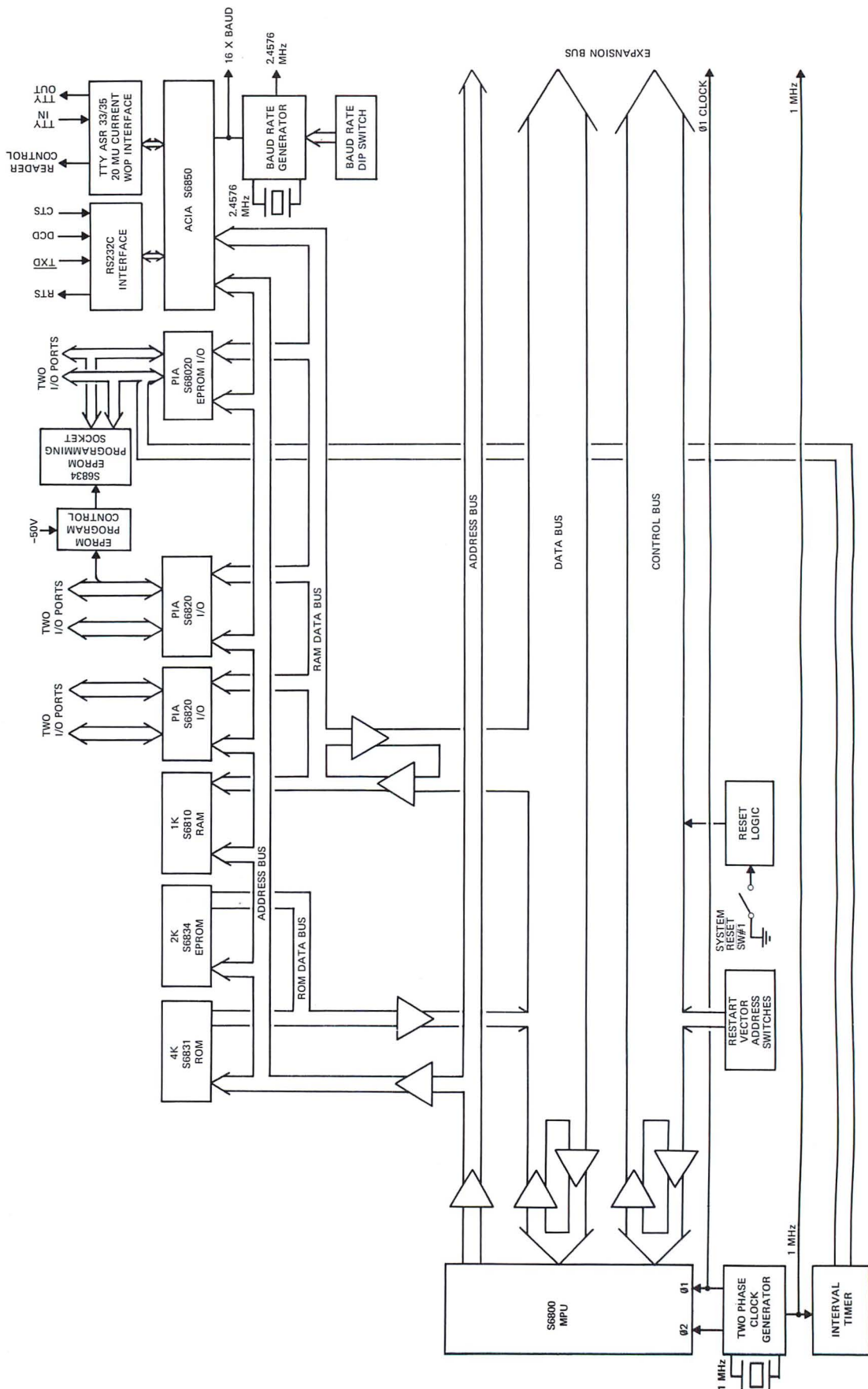
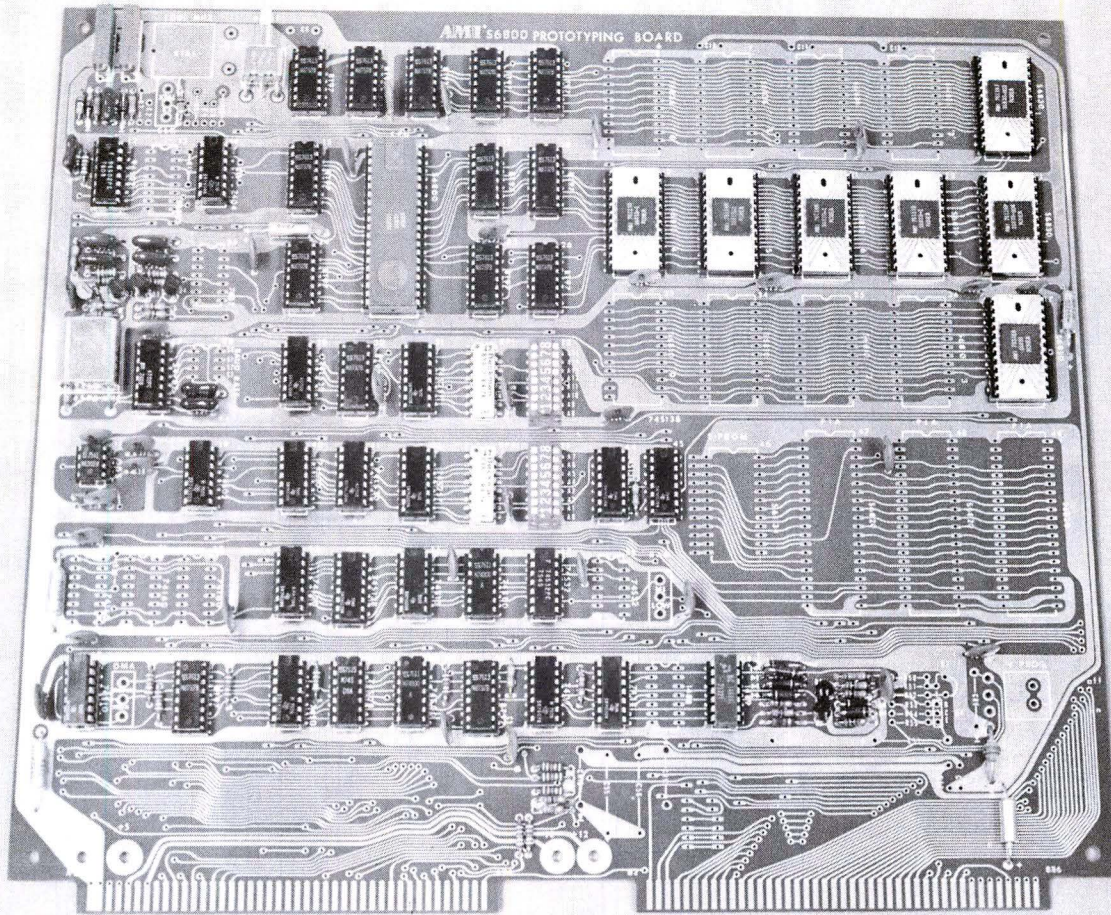


Figure 1. EVK Series Microcomputer Board



MAJOR EVK MICROCOMPUTER FEATURES

The common denominator EVK Microcomputer PCB provides the following on board major features when fully populated with hardware and software including options;

- 4K Bytes S6831 ROM memory (2K using S6831 ROM's)
- 2K Bytes S6834 EPROM memory
- 1 K Bytes S6810 Static RAM memory
- On board S6834 EPROM programming
- Six 8 bit PTA I/O ports
- 20 ma serial TTY current loop port interface
- RS232C EIA serial I/O port
- Switch selected baud rates to 19,200 bauds
- 1 MHz crystal or variable one shot MPU clock
- 5 crystal controlled timing signals available at PCB interface
(2.4756 MHz 1MHz 16x baud rate, 100 μ s & 1 ms)
- Interrupt internal timing (100 μ s & 1 ms)
- Switch selectable MPU restart address
- 200 ms Power On Reset delay
- 3 DMA modes (HALT MPU, CYCLE STEAL & MUX)
- TTY PROTO Monitor System resident in ROM
- RS³ ROM Subroutine Library resident in ROM
- ROM Resident Assembler — option
- Up to 40 ma @ 0.4V external bus loading
- 8T97 three state MPU bus drivers
- All MPU signal lines isolated & buffered
- System expansion via two 86 pin connectors

TYPICAL EVK MICROCOMPUTER APPLICATIONS

The EVK Microcomputer board allows the hardware development engineer, the logic designer, the programmer, the systems engineer, the mathematician, the scientist, the chemist or the hobbyist to have a complete working Microcomputer system, including development software by adding a low cost power supply and an ASR 33 TTY to the EVK Microcomputer board. The EVK series of Microcomputers boards allows the owner/user to use one of these boards to:

- Evaluate the complete set of AMI's family of Microcomputer IC's at a low investment of time & money — no design time is required.
- Serve as a general purpose Microcomputer for low volume systems to which the systems engineer can easily add additional I/O ports and memory.
- Serve as a low cost quick turn around prototype system to evaluate total system mechanization concept (hardware & software) and market acceptance prior to committing to a custom design system for large volume production.
- Serve as a low cost minimal 6800 Microcomputer application software development system.
- Serve as a low cost general purpose Microcomputer to run numerous application software programs.

Figure 2. AMI S6800 Prototyping Board Schematic Diagram

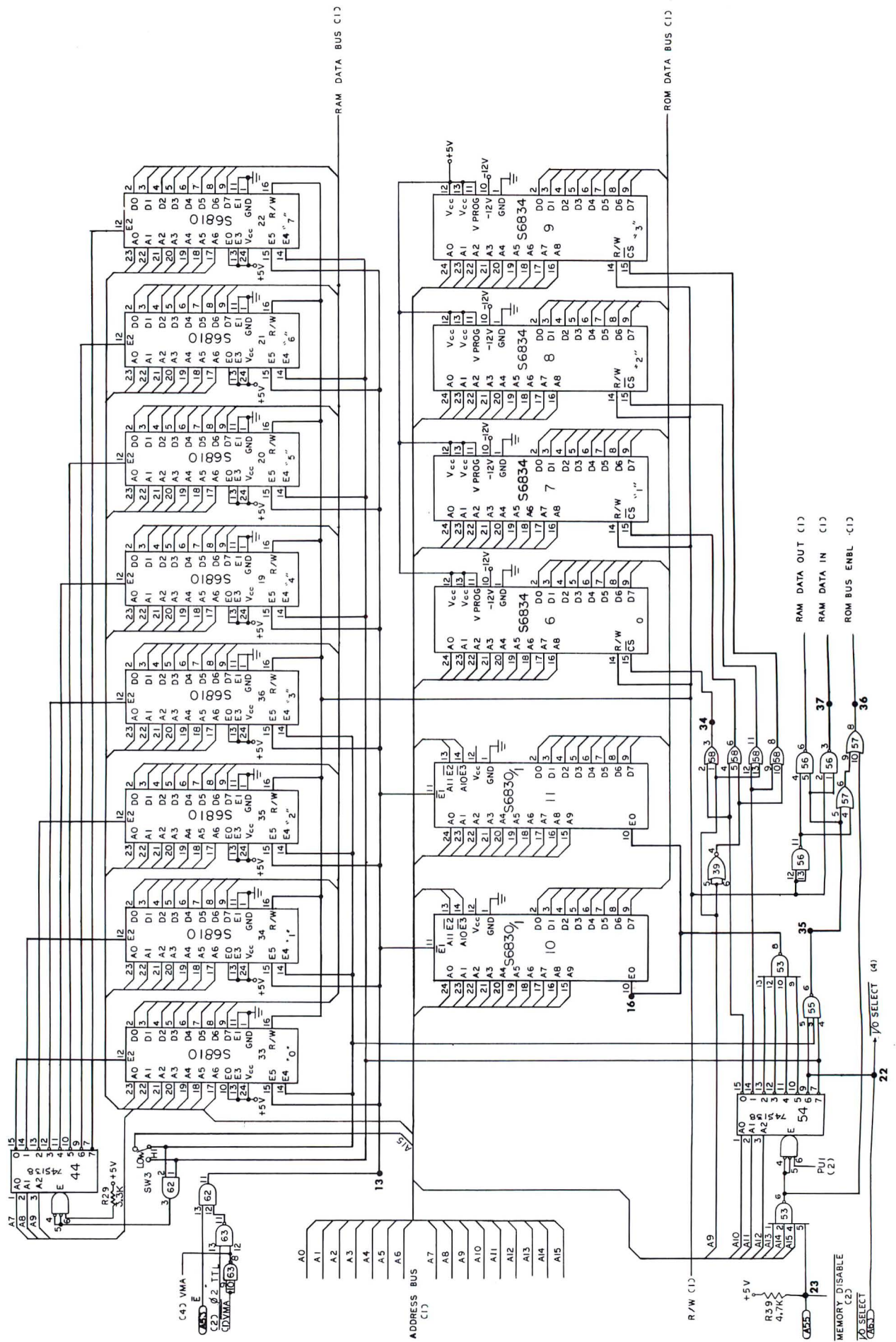


Figure 4. AMI S6800 Prototyping Board Schematic Diagram

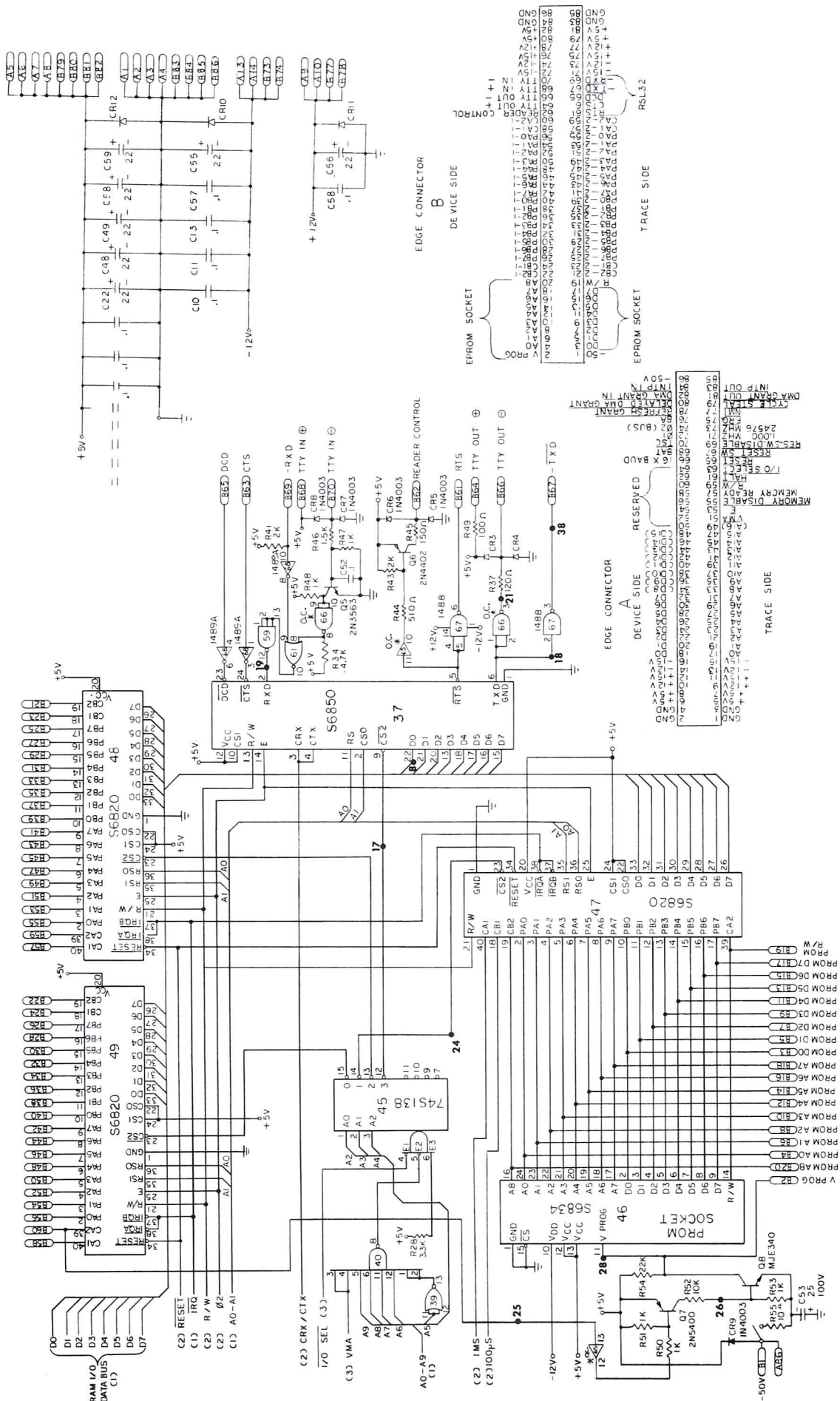


Figure 5. AMI Prototyping Board Schematic Diagram

EVK MICROCOMPUTER FUNCTIONAL DESCRIPTION

FUNCTIONAL CONFIGURATION

The following functional description is directed towards the fully populated EVK 300 Microcomputer board and is functionally applicable to the complete series of EVK boards limited only by the degree of board hardware-software population.

No attempt will be made to functionally describe the characteristics of AMI's Microcomputer IC chip set as this was undertaken in the first article entitled AMI 6800 Microcomputer Chip Set published last month in *INTERFACE AGE*. Instead, we will describe the general architecture of the EVK Microcomputer board and its general characteristics in order to provide an insight into EVK board utilization.

GENERAL ORGANIZATION

The EVK Microcomputer functional configuration is composed of the following major functional sections: MPU, clock, internal timer, memory, EPROM programmer, internal bus, expansion bus, I/O bus, I/O, and control logic sections. This functional inter-relationship is shown in Fig. 1, EVK Microcomputer Functional Block Diagram while the detailed logic and circuit information is shown in Fig. 2, 3, 4, & 5, EVK Microcomputer Logic Diagrams.

MPU — The MPU is mechanized with AMI's S6800 Microprocessor chip. All MPU data address and control lines are buffered, and in addition are available at the board edge connector.

MPU TWO-PHASE CLOCK — The basic MPU two phase clock is derived from a 96S02 dual one-shot (IC12) connected either in a regenerative feedback loop or driven by a 1 MHz crystal controlled oscillator circuit (IC14). Switch #SW 2 is used to select either the one-shot regenerative feedback or the crystal oscillator mode of operation. Phase one and two timing is controlled by potentiometers connected to the one-shot RC timing networks and controls the phase pulse widths. These two phase additive pulse widths determine the MPU clock rate when the one-shot regenerative feedback configuration mode is connected. In this regenerative feedback mode, MPU clock frequency may be adjusted from 300 KHz up to 1 MHz. The phase timing outputs of the one-shots in both modes of operation drive 2N5771-2N5772 transistor amplifier circuits which in turn drive the two phase clocks of the MPU. In addition, both clock phases are buffered and available at the board edge connector. The fixed frequency 1 MHz crystal oscillator circuit output is also buffered and available at the board edge connector.

The two phase clock can be halted in either phase 1 or phase 2 for cycle-steal, DMA or slow memory applications. Phase 1 is halted (held HIGH) by driving the CYCLE STEAL control line LOW. Phase 2 is halted (held HIGH) by driving the MEMORY READY line low. Because the S6800 internal registers are dynamic and must be refreshed periodically CYCLE STEAL and MEMORY READY line outputs to the one-shots cannot be held LOW for more than 5 μ s. This time limit protection, regardless of control input conditions, is provided by open collector 7407 (IC65) Hex non-inverting

drivers, disconnect diodes and one-shot RC pull-up timing networks.

INTERNAL TIMER — A crystal controlled interval timer provides 100 μ s and 1 ms time periods for interrupting the MPU for real time clock applications. The 1 MHz crystal clock output drives a three decade divide-by-ten 74160 counters (IC50, 51, & 52) which in turn provide the 100 μ s and 1 ms time intervals. The 100 μ s time interval pulse sets bit 7 of I/O address FBC7 via the S6820 PIA (IC47) while the 1 ms time interval pulse sets bit 7 of I/O address FBC5 via the S6820 PSA. These two time interval signals are used for timing EPROM programming.

MICROCOMPUTER BUS ARCHITECTURE — The EVK Microcomputer in essence has three sets of busses, namely the MPU bus, the Microcomputer bus and the on board memory-I/O bus. Each bus set consists of an 8-bit bidirectional data bus, a 16-bit unidirectional address bus and a control bus. The MPU bus is isolated from the Microcomputer bus in order to keep MPU signal loading to a minimum. The on board memory-I/O bus is isolated from the Microcomputer bus in order to assure that the on board memory and I/O devices do not load down the Microcomputer bus. As a result of this load isolation 40 ma drive current is available to drive external expansion hardware. The bus isolation buffers are non-inverting 3-state hex buffers (8T97). All of the controls to and from the S6800 are available at the board edge connector. This allows the user complete access and control of the MPU. Bus logic polarity is the same on all three busses (logic true = voltage high = "1"). The enable control signals to the MPU are always active. Control signals for the address bus are gated by the DMA GRANT line. The data bus is controlled by the DMA and R/W Lines.

MEMORY — The on board memory includes 1K bytes static RAM, 4K bytes ROM and 2K bytes EPROM.

MEMORY ADDRESS ASSIGNMENTS — Address assignments have been made such that all components on the card can run in the upper 8K bytes of memory. An address assignment map is shown in Figure 6.

Address decoding is made by use of three 74S138 one-of-eight decoders (IC 44, 45, 54). The first decoder (IC 54) selects one 1K-byte block of the upper eight 8K-bytes of memory. The output of this decoder is for RAM, I/O, ROM, or PROM enable lines. The second decoder (IC 44) selects one of eight RAM memory chips. The third (IC 45) selects I/O devices on the board.

A MEMORY DISABLE line is available at the Bus edge connector. This line, when LOW, deselects the first address decoder disabling all I/O and memory devices on the board. An I/O ENABLE line is derived from the first address decoder and is available at the Bus edge connector. It must be noted that I/O ENABLE on the backplane is not valid when MEMORY DISABLE is LOW.

READ ONLY MEMORY — The Prototyping Board has assigned locations for two 1K byte S6830 ROMs and for four 512 x 8 S6834 EPROMs. The ROM circuits are designed such that the locations will also accept two 2K byte 16K ROMs (S6831). Thus, maximum memory allocation for ROM and EPROM is 6K bytes. The prototyping operating system program (PROTO) is assigned to the ROM with a starting address of F000.

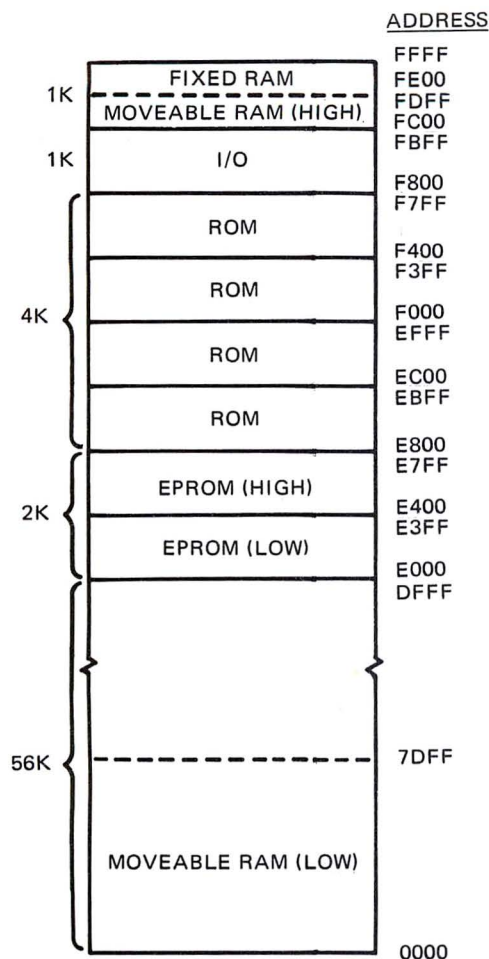


FIGURE 6. MEMORY ASSIGNMENT MAP FOR THE AMI PROTOTYPING BOARD

The four EPROM locations may contain any user program. Execution can start from beginning EPROM location either by selecting EPROM starting address of E000 in the restart switches or by branching to that address using the "G" command in the PROTO program.

RANDOM ACCESS MEMORY — The RAM is divided into two parts, 512 bytes fixed in the highest memory locations and 512 bytes of moveable memory.

Since the highest memory locations (FFFE, FFFF) are used for restart address, the address circuits disable the RAM using a memory disable line and force the 16 bit switch address on the data bus whenever a Reset occurs. This allows the user to vector to any address as his restart address.

The PROTO program assigns restart vectors for IRQ, NMI, and SWI whenever it is started (usually via Reset). It is therefore important to note that the user program must do the same thing if he does not use PROTO and restarts from a power down mode.

The stack pointer is assigned to address FF8F in PROTO. This allows the remaining RAM to be used as stack if so desired.

A switch option allows 512 bytes of RAM to be relocatable. When in the upper portion of memory, the RAM is assigned to addresses FC00 to FDFF making all 1K-bytes of RAM on the board contiguous (FC00 to

FFFF). When in the lower portion of memory, the 512 bytes are addressed whenever A9 and A15 are not true (0000 — 01FF for example). It is thus recommended that RAM be assigned to the low address only if the user does not add other RAM to his development system.

I/O — On board I/O includes parallel PIA I/O ports and serial ACIA TTY and RS232C I/O ports.

PARALLEL I/O — Three S6820 PIA's give the user a wide range of I/O flexibility. The PIA's are assigned addresses as shown in Table 2. Interface pins of these devices are directly connected to the I/O edge connector. The CA2 pin for the PIA at addresses FBC4 is also connected to the VPROG input (pin 11) to the EPROM socket (IC 46) through a +5V to -50V driver. The user is cautioned to use this line such that it will not interfere with his I/O function if programming an EPROM. For example, if the CA2 line is connected to an external control function, this function may be erroneously activated while programming an EPROM.

TABLE 2. I/O ADDRESS ASSIGNMENT

I/O PORT	ADDRESS	ASSIGNMENT
S6850 ACIA	FBCE	Serial I/O — TTY
	FBCF	Status/Read Control/Write
S6820 PIA 1	FBC8	Unassigned
	FBC9	Peripheral Register A
	FBCA	Control Register A
	FBCB	Peripheral Register B
S6820 PIA 2	FBCB	Control Register B
	FBC0	Keyboard/Unassigned
	FBC1	Peripheral Register A
	FBC2	Control Register A
S6830 PIA 3	FBC3	Peripheral Register B
	FBC3	Control Register B
	FBC4	PROM Burner
	FBC5	Peripheral Register A
	FBC6	Control Register A
	FBC7	Peripheral Register B
	FBC7	Control Register B

SERIAL I/O — One S6850 ACIA allows the system to communicate bi-directionally with serial data I/O peripherals such as a TTY. A baud rate generator generates all standard communication frequencies by switch selection. This frequency operates independently of the system clock so the MPU frequency can be changed without altering the I/O clock rate. See Table 3 for switch setting and associated frequencies. A 20 mA current loop interface and an RS-232 interface are both available at the I/O edge connector.

Address assignments for the ACIA are given in Table 3, "Bit Rate Generator Switch Settings."

EPROM PROGRAMMER — A unique feature of the Prototyping Board is its ability to program AMI S6834 EPROMs. A third PIA latches the address and data information for programming the EPROM. The EPROM socket programs only the S6834 EPROM, however, an adapter plug is available to also program the AMI S5204A EPROM. Except for the VPROG input, all address, chip select, R/W and data I/O pins on both EPROMs are completely TTL compatible and are driven directly from the PIA outputs. The outputs are also available on the I/O edge connector for convenience in using another EPROM programming socket.

TABLE 3. BIT RATE GENERATOR SWITCH SETTINGS,

0 = CLOSED, 1 = OPEN

SW POSITION				BIT RATE
4	3	2	1	
0	0	0	0	19,200 baud
0	0	0	1	0 baud
0	0	1	0	50 baud
0	0	1	1	75 baud
0	1	0	0	134.5 baud
0	1	0	1	200 baud
0	1	1	0	600 baud
0	1	1	1	2,400 baud
1	0	0	0	9,600 baud
1	0	0	1	4,800 baud
1	0	1	0	1,800 baud
1	0	1	1	1,200 baud
1	1	0	0	2,400 baud
1	1	0	1	300 baud
1	1	1	0	150 baud
1	1	1	1	110 baud

Programming is achieved by pulsing the VPROG pin with -50 volts through the CA2 line of the PIA at address FBC4. This line drives the transistor that gates the -50 volt source to the VPROG pin. The -50 volt source is switched ON or OFF via the VPROG switch.

CONTROL — The Microcomputer control section includes system reset logic, addressable reset logic and DMA control logic. In addition, an external logic circuit may be added to provide selection between RUN and single step modes.

RESET — The Reset circuit provides a timed reset for Power On Reset timing and for the Reset switch. The circuit is a timed oscillator which provides a 200 ms reset pulse.

RESTART — The starting address of an S6800 is FFFE/FFFF. The contents of these memory locations are put into the Program Counter register each time the MPU is reset. The Evaluation Board traps the FFE/FFFF addresses and puts the contents of the two 8-bit switch sets (IC 32, 43) on the data bus for each address and disabling memory, then gating the first set of switches to the Data Bus during FFFE time and the second set during FFFF time. The user is thus allowed to select any restart address by simply selecting a two byte address on the 16 bits of switch settings. The two DIP switches may be replaced with four hex thumb-wheel switches mounted on a front panel and interconnected via a flat ribbon cable and DIP plug connectors providing front panel Hex restart control.

DMA — Three types of DAM implementation are possible on the Prototyping Board, a halt processor mode, a cycle steal mode and a multiplex mode. A switch selects these DMA modes. The switch must be in the DMA position for the multiplex DMA mode. A delayed clock gives the DMA GRANT line to the bus after the "Data Hold" time has passed for a multiplexed type of DMA operation. The control lines for the halt processor and cycle steal modes are available at the Bus edge connector.

RUN/HALT & SINGLE STEP EMBELLISHMENTS — A simple low cost three IC RUN/HALT-Single Step Instruction logic may be added external to the EVK

board to provide these capabilities if required. Figure 7, RUN/HALT & Single Cycle Instruction Logic Diagram and Figure 8, Single Step Timing Diagram depicts this added logic mode.

POWER REQUIREMENTS

The EVK board is mechanized so that nominally only a +5 volt @ 3.5 amp power supply is required. A -12 volt supply is required when using S6834 EPROM ICs. In addition, a -50 supply is required when programming these EPROMs. The RS232C Interface requires both the +12V and -12V supplies for proper operation. The following is the total power and voltage level requirement for a complete operational EVK 300 Microcomputer board;

+5V @ 4 Amps
 -12V @ 150 ma
 +12V @ 50 ma
 -50V @ 50 ma

SOFTWARE

The EVK 300 Prototyping Board Software is comprised of a TTY Operating Program (PROTO) and is supported by a ROM Subroutine Library (RS)³.

PROTO— The EVK 300 is supplied with a prototyping operating system program (PROTO). The program resides in ROM with a starting address of F000. The various routines within PROTO are called by entering via the TTY keyboard one of the commands. A command consists of one character command identifier followed by additional parameters, if needed, separated by blanks or commas. All commands end with a carriage return. Since no action is taken before the carriage return, an input line may be deleted by the use of the TTY ESCAPE key. The PROTO program operates on the following commands:

- L Load Memory from TTY paper tape (HEX Format)
- P Punch a Memory location to TTY paper tape (HEX Format)
- S Set (write) Memory to a given value
- D Display the contents of a memory location in HEX
- G Go to user program at specific address and begin program execution
- R Print contents of MPU C, B, A, X, P & S register on the TTY
- B Burn (program) an EPROM from Memory location indicated
- V Verify the contents of an EPROM with a specified memory location
- I Input (copies) contents of EPROM in the programming socket into memory.
- M Move a specific block of memory to a designated location
- E End of transmission (EOT) character terminates the record and punches EOT on paper tape.

The commands will operate on a single character op code plus address parameters from the TTY keyboard.

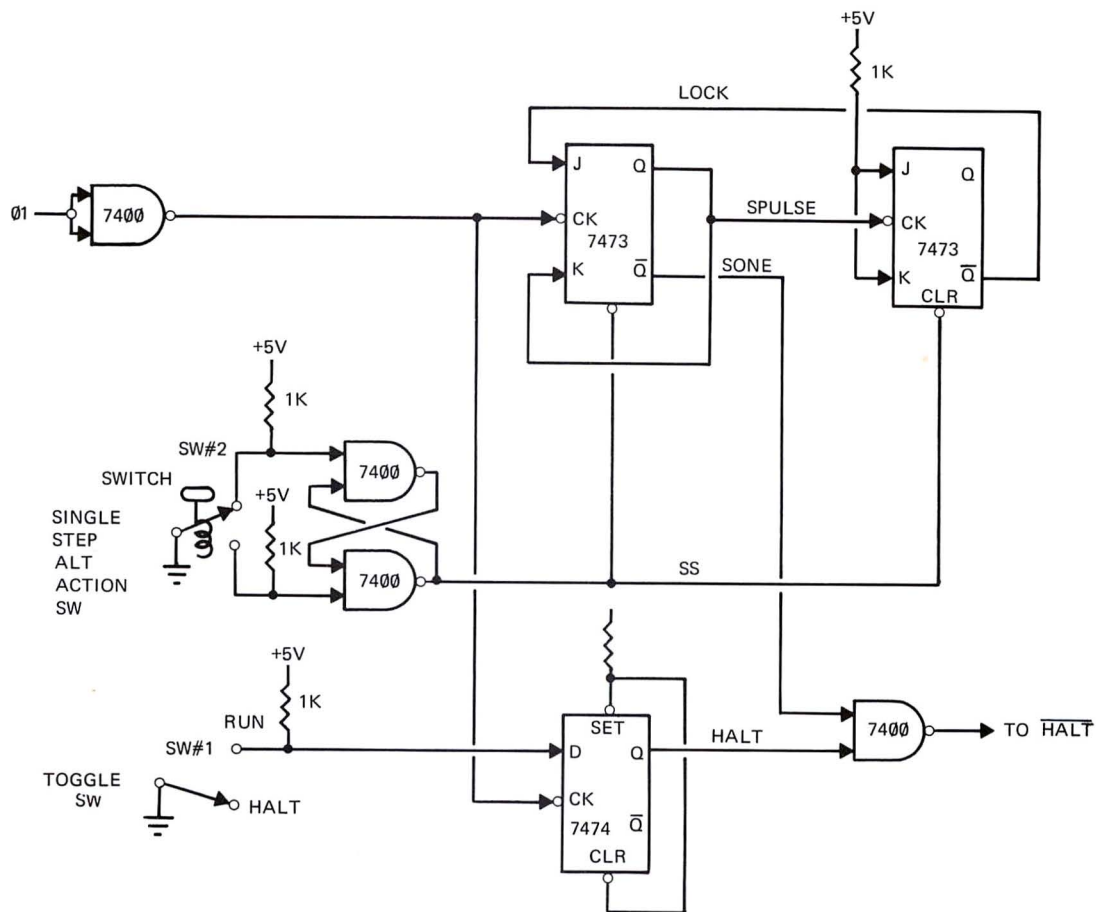


Figure 7. Run/Halt and Single Cycle Instruction Logic Diagram

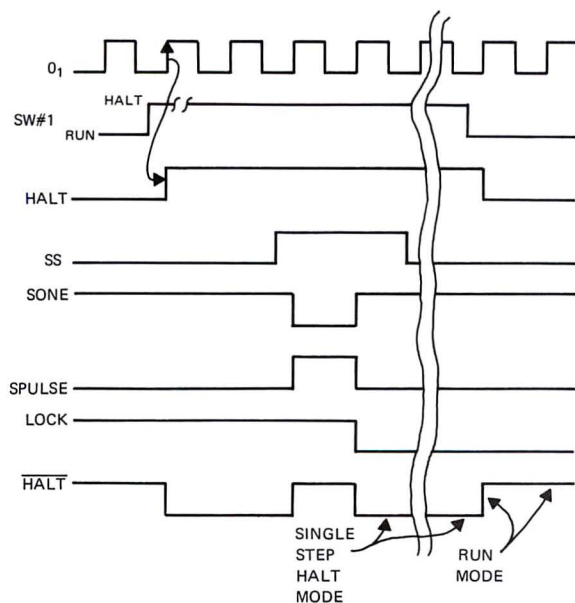


Figure 8. Single Step Timing Diagram

(RS)³ SUBROUTINES — The 2K X 8 ROM provided with the PROTO prototyping system includes a set of (RS)³ subroutines with a slightly different linkage from the standard (RS)³ form, although the calling sequence is the same. In particular, the provision for additional subroutines in the of other (RS)³ ROMs is limited to a total of 127 subroutines. The first additional (RS)³ ROM address must be placed in RAM location FFF4 (which can be set via the Set Memory command or modified by an initialization code in a user program). Also, since it is incorporated into a larger program, the whole of which very nearly fills the 2K bytes of its ROM, the (RS)³ part of the ROM does not start on an even page boundary, making it awkward for isolated use. However, the 24 subroutines included in this ROM are available to user program calls with the SWI calling sequence, as described.

The ROM Subroutine Library (RS)³ operates on a single SWI (3F) command and a second byte of offset giving the S6800 an additional set of two-byte instructions. Specific subroutines (offsets) are as follows.

SUBROUTINE INDEX	MNEMONIC	FUNCTION
0	PUSHALL	All registers are pushed on to user stack.
1	POPALL	All registers on user stack are loaded into MPU.
2	TXAB	Contents of Index Register are transferred to A & B Accumulators.
3	TABX	Contents of A & B Accumulators are transferred to Index Register.
4	XABX	Contents of A & B Accumulators are exchanged with contents of Index Register.
5	PUSX	Contents of Index Register are pushed onto user stack.
6	PULX	Index Register is loaded with contents of user stack.
7	ADDXAB	Contents of Index Register are added to contents of A & B Accumulators. Sum is in A & B Accumulators.
8	ADDABX	Contents of A & B Accumulators are added to contents of Index Register. Sum is in Index Register.
9	ADDAX	Contents of Accumulator A are added to contents of Index Register. Sum is in Index Register.
10	ADDBX	Contents of Accumulator A are added to contents of Index Register. Sum is in Index Register.
11	SUBXAB	Contents of Index Register are subtracted from contents of A & B Accumulators. Remainder is in Accumulators A & B.
12	SUBABX	Contents of Accumulators are subtracted from contents of Index Register. Remainder is in Index Register.
13	SUBAX	Contents of Accumulator A are subtracted from contents of Index Register. Remainder is in Index Register.
14	SUBBX	Contents of Accumulator B are subtracted from contents of Index Register. Remainder is in Index Register.
15	P2HEX	Two Hexidecimal Characters (one MPU byte) are printed on the TTY.
16	P4HEX	Four Hexidecimal Characters (two MPU bytes) are printed on the TTY.
17	PRINTA	ASCII Character designated is printed on TTY.
18	PMESS	Message designated is printed on TTY.
19	VALAN	Character (byte) is checked to see if it is a valid alpha/numeric character.
20	INPUTA	ASCII Character at TTY is input to MPU.
21	CONHB	ASCII Character string is scanned looking for a valid Hexidecimal number. Binary equivalent is returned in Accumulators A & B.
22	INDEX	Contents of Accumulator A are multiplied with the contents of Accumulator B and the product is added to the contents of the Index Register.
23	MUL8	Contents of Accumulator A are multiplied with the contents of Accumulator B. Product remains in both Accumulators.

S6800 MICRO ASSEMBLER/DISASSEMBLER (MA/D) —

An optional ROM resident Micro Assembler/Disassembler is available for the EVK Microcomputer board at an additional cost of \$30.00. Where this option is provided for those applications it may be desirable to debug programs using the

mnemonic instruction codes instead of hexadecimal values. MA/D is designed to accomplish this by interfacing with a user via a keyboard and display (TTY or equivalent). The required 6800 environment must include:

Character in routine at location	0
Character out routine at location	3
No. nulls after carriage return at location	6
RAM at locations	7 - 78 ₁₀

The I/O routines must transfer the characters in Register A and return with a RTS. It is expected that location 0 will just include a JMP to the actual character in routine, or, in the case of AMI's proto board:

```
00 SWI
01 FCB 20
02 RTS
```

The stack pointer must also be initialized before MA/D is entered. MA/D itself can execute from ROM, located anywhere in the system. MA/D may be started at its beginning address +2, in which case it will set up its environment for the AMI proto board.

After entering MA/D, the line length may be changed. The line length is in location 7 and is initially set to (20)₁₀ = 14 hex. The line buffer itself begins in location (58)₁₀ = 3A hex.

After displaying a header message MA/D prompts the user for a command by displaying MA/D's current location counter followed by a colon (:). The commands available to the user allow for disassembly of instructions in memory and assembly (mnemonic translation and operand insertion with relative offset computation) of instructions directly into memory.

MA/D is also very useful for writing short test programs. The instruction format for assembly is identical to the S6800 Assembler except:

- 1) operands must be in hexadecimal without the \$, and no more than four digits long
- 2) no symbols can be defined or referenced
- 3) relative addresses are specified as absolute addresses, the offset is computed
- 4) in those instructions having **both** direct and extended addressing modes, extended addresses must have at least three digits. Thus,
LDA A 10 assembles as 96 10
LDA A 010 assembles as B6 00 10
- 5) in those instructions not having a direct addressing mode, the operand may be two or more digits. Thus,
INC 10 assembles as 7C 00 10
- 6) an operand may be a single hex digit only if the op code indicates an A or B register, or immediate mode addressing. Thus,

```
INC 01      INC 1
LDA A 1     LDX 1
LDX #1
```

—are legal— —are not—

(This makes it easier to distinguish between, for instance, INC A and INC 0A.)

- 7) Anywhere a number is used, the construction 'character may be used instead, and is equivalent to the ASCII code for the character.

MA/D Command Summary

@newloc
@ newloc

The @ sign followed (immediately or with blank separator) by a hexadecimal address initializes the current location counter to the new address. MA/D automatically updates the location counter as instructions are assembled or disassembled.

\$count
\$ count

The \$ sign followed by a one or two digit (hexadecimal) count results in the disassembly of "count" instructions. Zero = infinity.

!address
! address

The exclamation mark followed by an address causes MA/D to call a subroutine at the given address. If the subroutine returns with the carry flag set, MA/D will print "????".

!

Exclamation mark with no address given causes MA/D to call the subroutine starting at the current location.

"string

Assembles the ASCII characters following the double quote mark into successive bytes of memory starting at the current location. The current location is updated.

xx
x
'character

A one or two digit hexadecimal number is placed into the current location, and the current location is incremented by one. A single quote mark followed by a single character causes the ASCII code for that character to be placed in the current location.

This command may appear several times on the same line, the numbers or quoted characters separated by spaces or commas.

&address,count
& address,count
&address count
& address count

Ampersand followed by a hexadecimal address and count (from 1 to 4 digits each) causes "count" bytes to be moved from "address" to the current location. On completion, the current location is incremented by "count".

<RETURN>

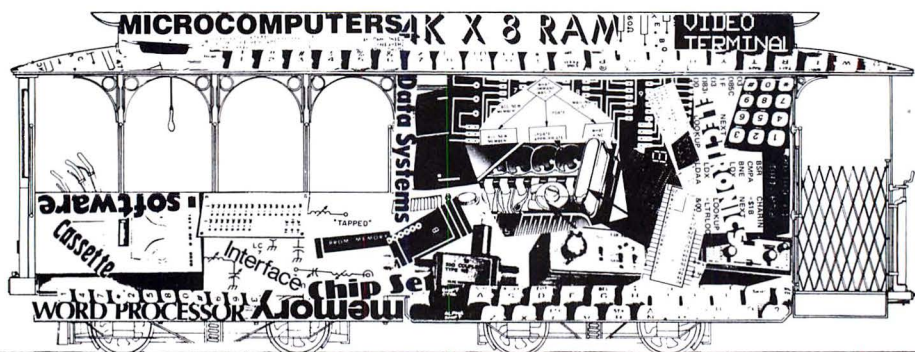
Carriage return is equivalent to \$01, disassemble a single instruction.

The commands to MA/D are buffered and not processed until the <RETURN> key is depressed. The <BACKSPACE> key can be used to delete the last character input. If errors are detected on user input the line is ignored, ??? is displayed, and another prompt is issued.

The default command is "assemble" and MA/D, if not recognizing the input as one of the following commands, generates the machine code for the instruction mnemonic.

Next month we will publish the complete PROTO Assembly Listing for the EVK Microcomputer board.

```
>
>G E002
A.M.I. 6800 MICRO ASSEMBLER/DISASSEMBLER — 1.0
(C) 1976, A.M.I.
002A:@80
0080:"THIS IS LOOP NO.
0090:"0000
0094:04
0095:LDA A 93
0097:INC A
0098:STA A 93
009A:CMP A #3A
009C:BNE 110
009E:LDA A '0
00A0:@9E
009E:
009E-> 96 LDA A 30
00A0:@9E
009E:LDA A #'0
00A0:STA A 93
00A2:LDA A 92
00A4:INC A
00A5:STA A 92
00A7:BRA 110
00A9:@110
0110:LDX #0080
0113:LDA A 00,X
0115:CMP A #04
0117:BEQ 120
0119:JSR E003
011C:@119
0119:JSR 0003
011C:INX
011D:BRA 113
011F:NOP
0120:LDA A #0D
0122:JSR 0003
0125:LDA A $0A???
0125:LDA A #0A
0127:JSR 0003
012A:JMP 095
012D:@95
0095:$3
0095-> 96 LDA A 93
0097-> 4C INC A
0098-> 97 STA A 93
009A:195THIS IS LOOP NO.0001
THIS IS LOOP NO.0002
THIS IS LOOP NO.0003
THIS IS LOOP NO.0004
THIS IS LOOP NO.0005
THIS IS LOOP NO.0006
THIS IS LOOP NO.000
>
>
```

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- Floppy Disc Systems for Personal Computers
- Computer Games: Alphanumeric & Graphic
- Computers & Systems for Very Small Businesses
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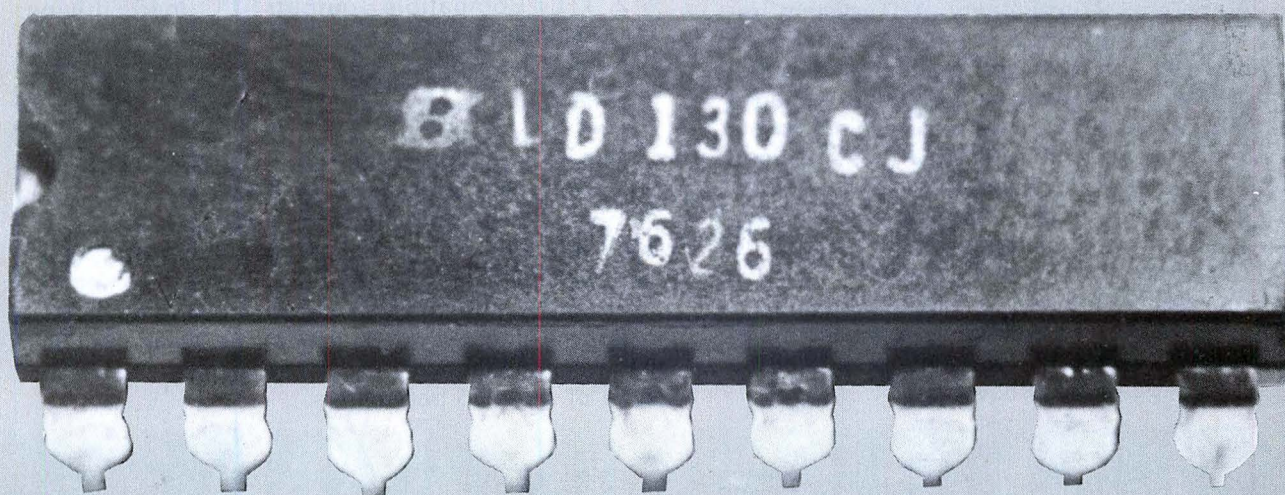
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Hardware Report:

Build a 3 Digit A/D Converter for Your Microcomputer



By Roger Edelson

For the next two months Hardware Report will cover the Siliconix LD130 Monolithic CMOS A/D Converter. This Device is admirably suited to provide a general purpose analog-to-digital (A/D) interface for your microprocessor system that requires only one chip (the LD130), and a minimum of additional components. This device will provide a 3-digit bi-polarity (both positive and negative — effectively doubling the conversion range) A/D conversion at rates up to 60 samples per second. Using a two transistor decode scheme, which will be shown later, the inputs to the LD130 can be multiplexed to provide a number of channels of A/D conversion. However, using an input multiplexing scheme reduces the rate of conversions for any single channel by the number of channels multiplexed. In the case of a four paddle type game the maximum conversion rate for any one channel is, therefore, 60 divided by 4, or 15 conversions per second. This rate may be not fast enough in which case multiple LD130s could be used or, alternatively, a simpler A/D scheme, like a strobed one-shot could be used, as a 3-digit accuracy would not be required. Bearing this one limitation in mind, the LD130 is, however, ideal where 3-digit accuracy is required, and simplicity of hook up is desirable.

The LD130 combines both the analog and digital sub-systems of a 3-digit A/D system in a single monolithic CMOS I.C. The 'Quantized Feedback' conversion scheme, introduced by Siliconix, provides the LD130 with an Auto-Zero, Auto-Polarity A/D system requiring only a single reference voltage. External parts are minimized by the on-chip resistors and buffer amplifiers. These high impedance input and reference buffer amplifiers eliminate source loading errors providing the outstanding temperature coefficient and ratio operation inherent in this system. Break-before-make switching action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

Figure 1 shows the internal functional arrangement of the Siliconix LD130, as well as the connections of the external components. The pin configuration of the dual-in-line package is also shown.

Let's look at some of the features of this ± 3 -digit A/D converter.

1. Accuracy of 0.1% (of reading, not full scale) ± 1 count.
2. Auto-Zero (utilizes break-before-make switch action to insure that the input signal is not shorted to ground).
3. Auto-Polarity.
4. Low power consumption (25mw typical).
5. 1mv resolution (1.00V full scale).
6. Minimum of external components:
 - a. C_{AZ} (0.10 μ f) between AZ and Σ pins.
 - b. C_{INT} (0.033 μ f) between INT and Σ pins.
 - c. C_{OSC} (0.001 μ f) between OSC and digital ground.
 - d. $V_{REF} \cong 2.00$ V. must be provided.
 - e. ± 5 V supplies (@ 3ma) are needed.
7. Buffered Analog Input ($Z_{IN} > 1000M\Omega$)
8. Buffered Reference Input ($Z_{IN} > 1000 M\Omega$)
9. Internal Clock Oscillator (adjustable by selection of C_{OSC} or an external clock may be used.)
10. Overrange and Underrange Signals provided for Auto-Ranging.
11. Multiplexed BCD with inter-digit blanking (to minimize interface connections).
12. TTL Compatible outputs (1 load driving capability).
13. Sampling Rates from 1 to 60 Samples per second.

Table 1 gives the specifications of the LD130 chip. Note that many of the error sources are given as typical only. The typical values are given as a design aid *only*, and are neither guaranteed nor subject to production testing. In most cases your chip will conform to these values, and unless you really need to work close to the maximum error budget for some applications, they will not affect your usage of the chip. Let's discuss some of the chip parameters:

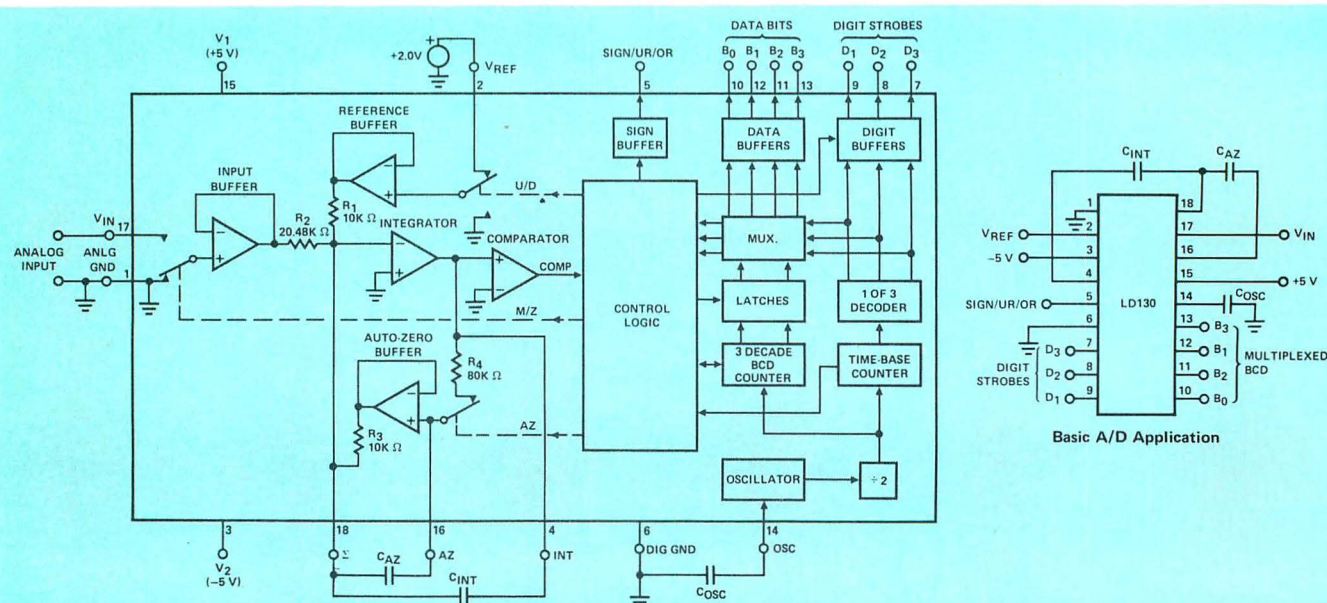
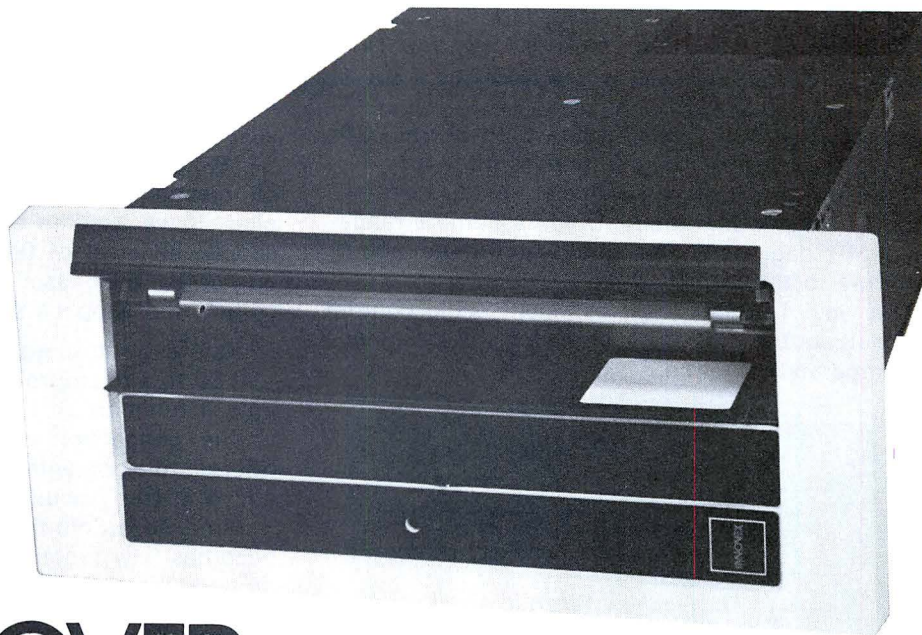


Figure 1. LD 130 — Functional Diagram



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	Kit	Assm.
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1. Linearity is given as a maximum error of 0.1% of the reading. That is quite a bit better than 0.1% of full scale which could give you an error of 1mv on a 1mv input signal (1.000v full scale) which would be a 100% error.

2. Noise is typically given as one third of the LSB (least significant bit) or roughly one count error.

3. The Zero temperature coefficient of zero setting is $10\mu\text{v}$ per degree/centigrade. If you assume a range of about 40 degrees/C this could contribute about $\pm 0.200\text{ mv}$ to the error budget.

4. The Gain Temperature Coefficient could contribute about another $\pm 0.03\%$ error for the assumed 40°C temperature change.

12-16. These items define the input and output parameters of the various logic and clock inputs. Note that the clock input requires 1ma of current in the high state. This is different than a standard TTL load.

17-18. Maximum limits for supply current. This device being a CMOS I.C. requires very little power.

19-20. These two parameters indicate the amount of rejection of noise contributed by the power supplies. If we assume a 200mv noise voltage on each supply, an error of 0.4mv will be contributed to the output. For this reason, in order to obtain maximum accuracy, the supplies should be fairly clean.

Before we discuss the application of the Siliconix LD130 to a microprocessor system let's take a look at how it functions.

The connection diagram of Figure 1 should be referred to along with the timing diagrams Figures 2, 3, and 4 in this discussion of functional operation.

Time Base Counter — The internal oscillator circuit becomes fully functional with an external capacitor to ground. The OSC input can be driven by an external oscillator (0 to V_i logic levels) if desired. A squaring circuit divides the oscillator frequency by two before it drives the BCD counter and Time-Base counter.

The two fundamental intervals of the sampling period, the Auto-Zero (AZ) and the Measure intervals, are established by the Time-Base counter as 1024 and 2048 clock periods respectively. The total sampling interval is then 3072 clock periods long. Since the internal clock is onehalf of the oscillator frequency, the sampling period is then 6144 (2×3072) oscillator periods. The Time-Base counter also divides the internal clock by eight. This division provides sets of eight clock periods (octets) which are used by both the data multiplexer as digit "ON" times and the control logic as U/D (Up/Down logic) duty cycle periods.

The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the LD130. In addition, it automatically establishes a second tracking reference voltage necessary for bi-polar A/D conversion.

The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amplifier to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and Integrator together in a closed loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods "Up" and 4 "Down" (See Figure 2).

If, for the moment, we ignore any error sources equilibrium of this closed-loop system is obtained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when the V_{AZ} , the Auto-Zero voltage, is equal to $-\frac{1}{2} V_{REF}$ since $R_1 = R_3$. Establishing V_{AZ} and storing it on C_{AZ} gives the U/D logic the capability of switching either a + or - reference current to the Integrator during conversion. Thus when U/D is "Up" the U/D switch is connected to ground, and the current to the Integrator is

$$I_1 - I_3 = \frac{0}{R_1} - \frac{V_{REF/2}}{R_1} = -\frac{V_{REF}}{2R_1}$$

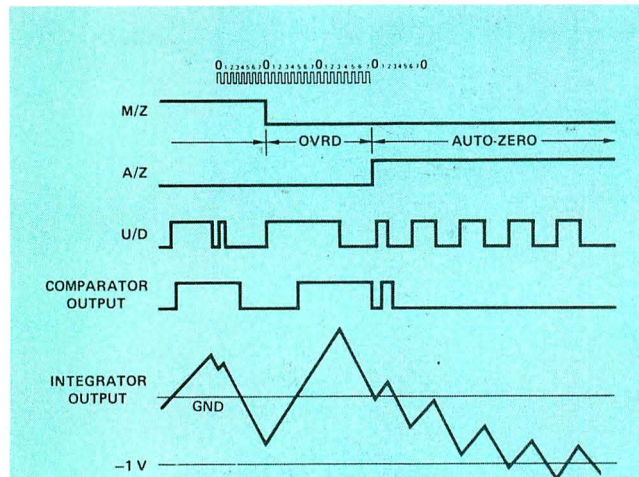


Figure 2. Auto-Zero Timing

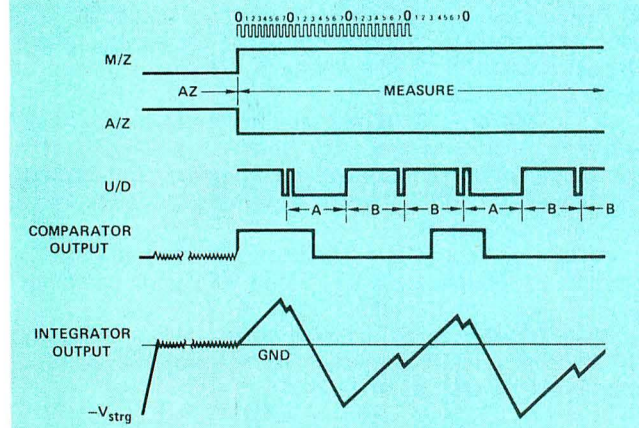


Figure 3. Measure Interval Timing

5. The normal mode noise rejection (NMR) is a minimum of 36db for a 60Hz noise frequency and a 24KHz clock. This gives a reduction of about 63 in the input noise. Later we will discuss a method for tuning the noise rejection of the LD130 to allow a maximum of over 70db noise reduction. This would give a reduction of over 3000 in the effect of the noise voltage.

6-9. These parameters define the input current for both the analog input and the reference input pins. At 70°C the input current will be less than 100pa which translates to >1000 megohms input impedance.

10-11. These two parameters define the clock conditions. Typically the clock frequency will be 30KHz with those components. The maximum clock frequency should be limited to $\sim 400\text{KHz}$. The duty cycle should be $50\% \pm 20\%$.

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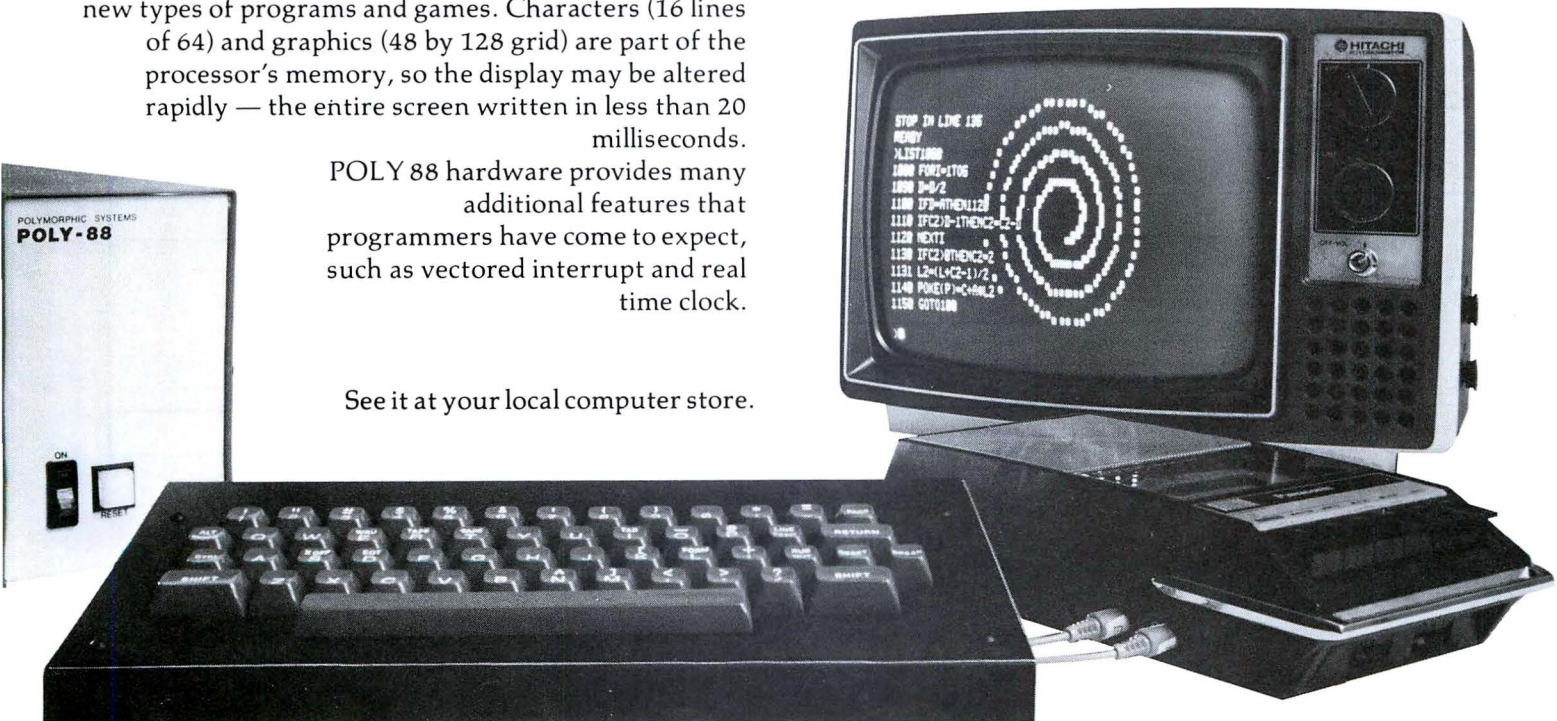
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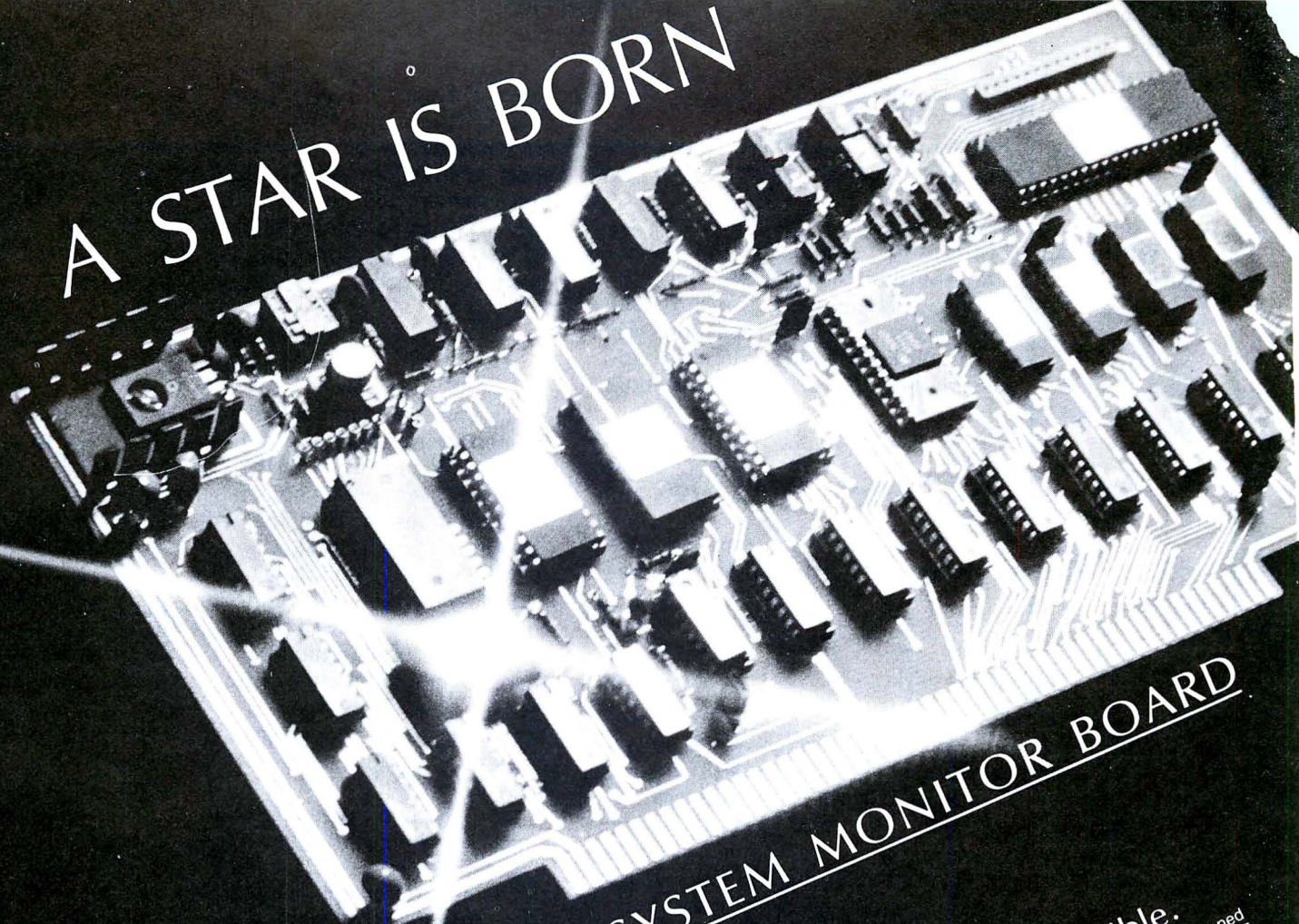
CHARACTERISTIC			MIN	TYP	MAX	UNIT	TEST CONDITIONS $V_1 = +5 \text{ V}, V_2 = -5 \text{ V}, V_{REF} = 2.000 \text{ V}$ $T_A = 25^\circ \text{C}, C_{INT} = 0.068 \mu\text{F}, C_{strg} = 0.1 \mu\text{F}$
1	GENERAL	Linearity			0.1	% rdg	
2		Noise		0.3		LSB	Peak-to-Peak noise apparent when going from one steady reading to another.
3		Zero T. C.		10		$\mu\text{V}/^\circ\text{C}$	$0 \leq T_A \leq 70^\circ\text{C}$
4		Gain T. C.		15		$\text{ppm}/^\circ\text{C}$	$0 \leq T_A \leq 70^\circ\text{C}$
5		NMR Normal Mode Rejection	36			dB	$f_{\text{series}} = 60 \text{ Hz}, f_{\text{osc}} = 24 \text{ kHz}$
6	INPUT	I_{IN} V_{IN} Input Bias Current		7		pA	$T_A = 25^\circ\text{C}$
7				90			$T_A = 70^\circ\text{C}$
8		I_{REF} V_{REF} Input Bias Current		7			$T_A = 25^\circ\text{C}$
9				90			$T_A = 70^\circ\text{C}$
10		f_{CLK} Clock Frequency		30		kHz	
11		D.C.CLK Clock Duty Cycle	30/70		70/30	%	
12		I_{INL} Clock Input Current Low			-1	mA	$V_{INL} = 1.0 \text{ V}$
13		I_{INH} Clock Input Current High			1		$V_{INH} = 4.0 \text{ V}$
14	OUTPUT	V_{OL} All Outputs			0.4	V	$I_{OL} = 1.6 \text{ mA}$
15		V_{OH} Sign, Digits	2.4				$I_{OH} = -400 \mu\text{A}$
16		V_{OH} Data Bits	2.4				$I_{OH} = -100 \mu\text{A}$
17	SUPPLY	I_1 Supply Current			6	mA	
18		I_2 Supply Current			-4		
19		$PSRR_1$ V_1 Supply Rejection		0.6		mV/V	
20		$PSRR_2$ V_2 Supply Rejection		1.4			

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When the U/D is "Down" the U/D switch is connected to V_{REF} and the current to this Integrator is:

$$I_1 - I_3 = \frac{V_{REF}}{R_1} - \frac{V_{REF/2}}{R_1} = \frac{V_{REF}}{2R_1}$$

If there is an error voltage developed in any of the amplifiers the V_{AZ} voltage will reflect this and change such as to eliminate any error current into the integrator null. Assume that we have a zero error current of $1 \mu a$ flowing into the null point. V_{AZ} will become V_{REF} per $-1 mV$ in order to null the integrator during Auto-Zero. In this "Up" condition the current to the integrator could become:

$$I_1 + I_3 + I_{ERROR} = \frac{0}{R_1} - \frac{V_{REF/2} - 1 mV}{R_1} - 1 \mu a = \frac{-V_{REF}}{2R_1} + 1 \mu a - 1 \mu a = \frac{-V_{REF}}{2R_1}$$

During the "Down" interval, $1 \mu a$ more current flows into the R_3 mode, and the current to the integrator is

$$\frac{V_{REF}}{2R_1}$$

You can see how nicely this system nulls out any amplifier or resistor errors so long as no parameter changes occur during the sampling interval. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.

Prior to the start of the Measure interval, the integrator output (which had been cycling around $-1V$) is brought back to analog ground, the comparator threshold. The system is now ready for a conversion.

The "Quantized Feedback" conversion system is characterized by a single phase Digitization interval in which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of the charge balance being supplied to the integrator by the analog voltage. The magnitude

$$\left(\frac{V_{REF}}{2R_1} \cdot \frac{6}{F_{CLOCK}} \right)$$

of the Quantized charge being fed back and its sign (+ or -) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval as shown in Figure 3.

The U/D logic is 'Up' one clock cycle and 'Down' 7 cycles for a high comparator output in the clock cycle preceding a set of eight cycles. This will be designated as duty cycle "A." With a low comparator output in clock cycle number 7 the U/D logic will be 'up' for 7 cycles and 'down' for one cycle in the following eight clock cycles. This is duty cycle "B". The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the 'up' state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is 'up' and decrements by each clock pulse when the U/D logic is 'down'. Consequently, the net count goes up 6 counts for a 'B' duty cycle and down 6 for an 'A' duty cycle.

Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be

negative if two 'A' duty cycles occur in succession and positive if two 'B' duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to "fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval. The determining equation of the LD130 is given as Count =

$$2000 \frac{V_{IN}}{V_{REF}}$$

While this seems to imply that the output is absolutely defined by this equation; however, there is a possible 5% variation in the LD130 chip resistor values and therefore V_{REF} must be adjustable over a 5% range. This equation does indicate that with a $V_{REF} = 2.0V$ the output will read directly in millivolts of analog input with 1.000 Volt full scale.

Following the count correcting override sequence; the contents of the BCD counters and sign flip-flop are loaded into the internal latches. Counter states of less than 80 or greater than 999 are decoded as under-range or overrange conditions respectively. The presence of an out-of-range signal gates a single pulse (one clock period) to the SIGN/UR/OR output during either D_1 or D_2 digit time (D_2 identifies overrange, D_1 under-range). The overrange condition also provides a visual signal by holding the digit strobe outputs low during the Measure interval. This holds the display off for $\frac{2}{3}$ of the sampling interval giving a blinking effect. The BCD data stored in the latches is continuously scanned every 24 clock periods (8 clock times per digit). Sign information appears at the SIGN/UR/OR pin coincident with the D_3 strobe. Interdigit blanking of the Digit Strokes is achieved by taking one full clock period from both the leading and trailing edges of the strobes. Thus the digit is on 6 clock periods while the BCD data for that digit appears for the full eight clock periods. Figure 4 shows the Data Output Timing.

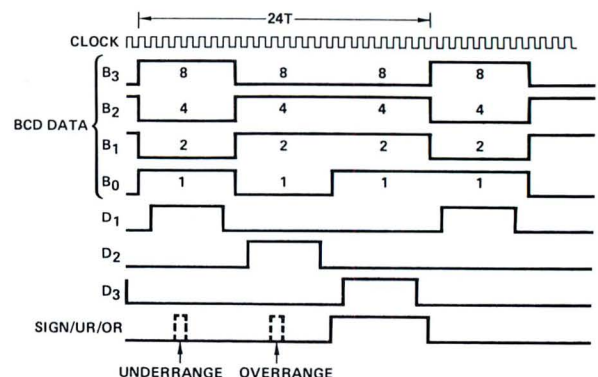
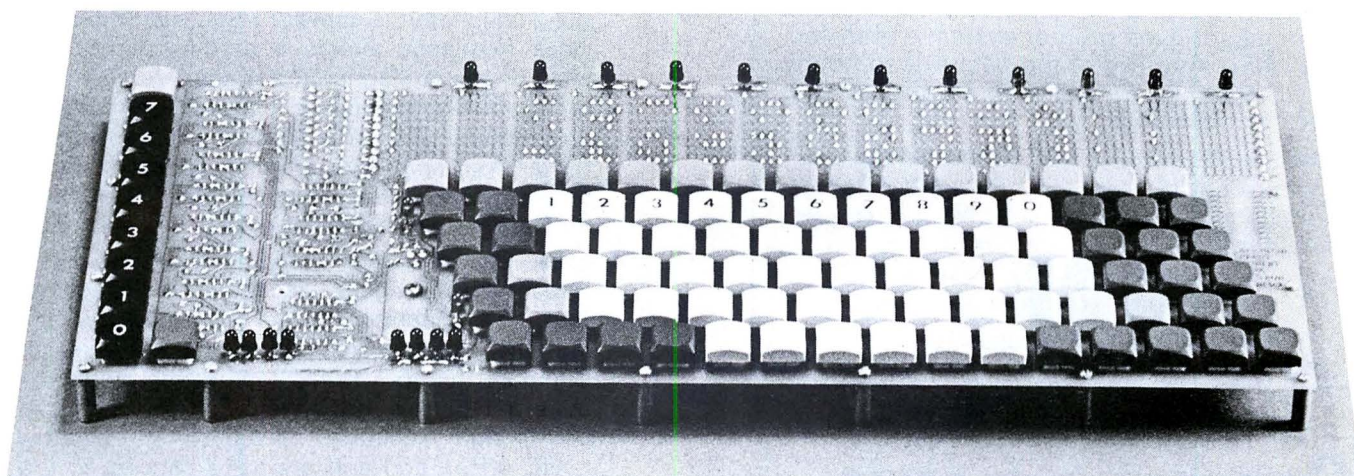


Figure 4. Data Output Format (Output = 769)

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Now that we have seen how the LD130 operates, let's discuss the advantages of Siliconix's "Quantized Feedback" conversion system particularly in comparison with the most commonly used integrating A/D system — Dual-Slope. These include:

1. Bipolar Conversion: Auto-Polarity is a natural outcome of a system which uses $+$ and $-$ reference currents. This is accomplished with a single reference voltage and a single full-scale adjustment.
2. One-Bit Wide Zero: Zero occurs naturally as a number between minus full-scale and plus full-scale in 'Quantized Feedback'. It then has none of the Dual-Slope zeroing problems which require special zeroing currents and counter delays leading to a "dead-band" around Zero of several bits.
3. Less Frequency Drift Sensitivity: "Quantized Feedback" does the conversion process while the analog input is applied. Thus, any drift in the clock frequency affects both the charge supplied by the analog input and the reference currents equally minimizing frequency drift as an error source. The Dual-Slope system integrates the analog input and reference currents during different time intervals making short term clock drift a possible source of error.
4. Less Sensitive To Comparator Errors: The "Quantized Feedback" technique only requires that the comparator resolve one part in six during the count-correcting override sequence. Compare this to a Dual-Slope which would require a 1 part in 1000 resolution for comparable 3-digit accuracy. Obviously comparator noise, offset, and drift are not a concern to the Siliconix system.
5. Fixed Conversion Time: The measure interval is fixed by the Time-Base counter. A data acquisition system once synchronized to the LD130 will not be tied up waiting for the new data. The Dual-Slope system has a conversion time proportional to the random analog input. This is particularly important to microprocessor users.

Next month we will conclude this article with a discussion of Operating Conditions, System Applications, and Microprocessor Interconnections.

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Microcomputer Design Aides

By Terry Benson
Applications Engineer
Intel Corporation



Learning to use and program microcomputers is becoming as important today as learning logical design fundamentals was a few years ago. As time goes on, use of microcomputers will eventually increase to a point that may even approach that of the pocket calculator. Learning about microcomputers will be as critical then as learning the multiplication tables is today.

In order to simplify the educational process, with the proliferation of microprocessors, more and more companies are producing "learning tools" and educational material supporting these microprocessors. Companies are also incorporating microprocessors into "hobby" computers. This makes it possible for many of us to have a personal computer — but how do we use it effectively?

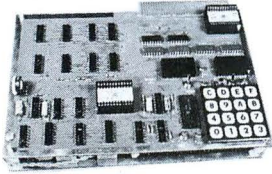
Many of these educational tools are dedicated for just that purpose and, consequently, are not practical

for use as a computer system. On the other hand, many of the hobby computers, which may be functional as a microcomputer system, assume a working knowledge of computers and thereby make it difficult for the beginner to effectively use the microcomputer. With these thoughts in mind we can consider some desirable features that should be included in a low cost design aid:

- 1) Newcomers to microcomputing should be able to learn how to use the microcomputer effectively.
- 2) For long term benefits, the design aid should be able to be used as a fully functional microcomputer system.
- 3) Most importantly, it should be convenient to debug programs and verify that the microcomputer system performs as desired.

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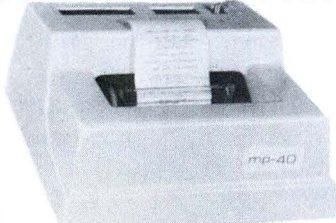
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58 INTERFACE AGE

USEFUL FEATURES OF A DESIGN AID

The novice may have had little, if any, formal computer programming training and may be struggling to learn the programming techniques that will make his microcomputer useful to him. In many cases he will want to single step through a program to see what happens within the microprocessor when the program decrements a register, gets data from an input port, or pushes data onto the stack. While features such as this are helpful in learning how a program functions, they can also be useful in debugging a program that a more experienced programmer may write. If the program doesn't work (and I imagine you've seen many of those), it is often helpful to be able to single-step through the suspected portion of the program while checking the values within the microprocessor registers. Whether you are learning about microcomputers or debugging a program, the ability to load and run the program in RAM (read/write memory) is essential. This allows you to make immediate program changes without having to erase and reprogram a PROM.

If these capabilities are available, the microcomputer system will be more useful to the user for a longer period of time. In order to highlight the importance of some of these features, let's discuss a typical program development cycle.

DEVELOPMENT CYCLE

The flow chart in figure 1 illustrates the steps that are involved in getting a microcomputer program working. These steps will be performed whether you are writing a game, designing an automated test system, implementing a controller, or designing any other microcomputer application. In the development flow chart as shown, it is assumed that the designer has a working microcomputer system. (Although this is not always a safe assumption, the hardware debug phase will be left for future discussions.)

Writing the program, block 1, may also consist of assembling or compiling the program into a machine readable format. In the lower cost design aids, the translation is performed by hand. After conversion, the machine language must be entered into the microcomputer system, block 2. The machine language can be entered in several different ways: program a PROM, read a paper tape into RAM, load RAM from toggle switches or hexadecimal switches or from a keyboard, etc.

In block 3, we begin to check out — or debug — our program. One optimistic approach is to start the program at the beginning and hope that it runs to the end. If it doesn't perform as intended, then you probably will follow the pessimist's approach — single step all or portions of your program. In fact, blocks 3 and 4 will probably require the majority of time in the overall software development cycle.

As each one of the bugs is found, a correction must be made to the program (block 5) and the verification cycle (blocks 3 and 4) repeated. The changes can each be entered in any one of the ways that the original program was entered, but it is during this correction phase that it is most desirable to have the program residing in RAM so changes can be easily implemented. Having

JANUARY 1977

the ability to specify the affected memory address and immediately entering the new or corrected data will simplify the entire debug cycle. If the program is operating in PROM, the PROM must be erased (or discarded) and reprogrammed for one more try — a rather time consuming operation if it must be done for each change.

After blocks 3, 4 and 5 have been reiterated enough times to have a properly running program, the program will have to be saved (block 6). Several alternatives for saving the program are available: the power can be left on (this might be a bit precarious); the object code can be stored on paper tape or a magnetic media; or, in cases where the program will be operating in a dedicated system application, a PROM can be programmed.

Through all of this we have been using the microcomputer system as a development system. During this development cycle, several desirable features have been mentioned. The ability to single step your program and observe the affect of each instruction can be invaluable in finding and correcting a program bug. The fact that RAM locations can be easily changed also enhances the program development cycle. One very desirable feature is the ability to copy the data in RAM *directly* to a PROM — a *built-in* PROM programmer.

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Few microcomputer systems have all of these desirable features incorporated into a single product. One product that does have these features is the Intellec*

PROMPT 80 System*, figure 2, recently introduced by Intel Corporation. The PROMPT 80 Personal Programming Tool is a self-contained microcomputer development system which supports the design of any 8080 system. It is a fully-assembled microcomputer that can be used for learning, debugging, and running 8080 programs.

The PROMPT 80 System uses an integral calculator-like hexadecimal keyboard for entry of machine language programs. (A teletype writer or CRT terminal may easily be added by simply connecting the appropriate wires.) The system is based on the SBC 80/10 Single Board Computer and includes 1K bytes of RAM, 3K bytes of ROM and 24 programmable parallel I/O (TTL) lines. A PROM programmer for the 8708/2708/2704 erasable PROMs is also included.

The following is a summary of the features that will facilitate both learning and debugging 8080 programs:

- 1) **Register Display** — all 8080 registers can be displayed, even while single stepping.
- 2) **Modify Register or Memory** — any 8080 registers or any of the 1K RAM locations can be modified.
- 3) **Single Step** — allows register data to be displayed (and modified for debugging purposes.)

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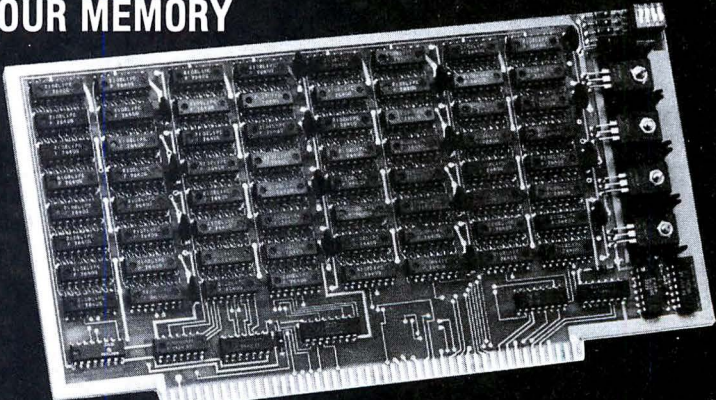
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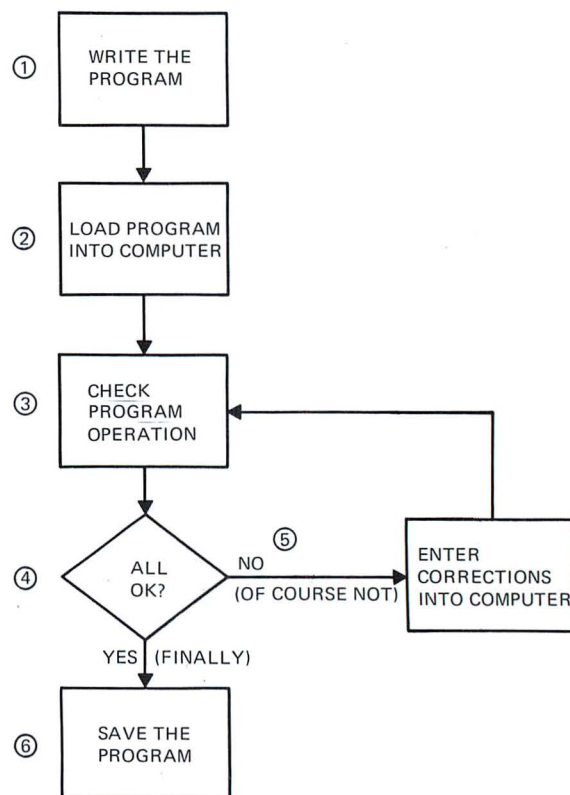


Figure 1. Program Development Flow Chart

- 4) **Break-points** — a program operating in RAM can be started and up to two break-points (program locations where you desire the program to stop) can be set.
- 5) **Program EPROM (2708)** — PROM programmer allows data to be copied from RAM to EPROM. (Data can also be transferred from EPROM to RAM.)
- 6) **Hex Calculator** — useful for adding and subtracting in the unfamiliar base 16.
- 7) **Built-in I/O Ports** — an 8-bit input port and an 8-bit output port are implemented on the control panel. These two ports along with 8 additional I/O lines are available on an I/O connector for external interface.
- 8) **Serial Port** — teletype of CRT terminal can easily be added.
- 9) **Expansion** — using a modular card cage (Intel SBC 604) and other SBC 80 expansion boards, memory and I/O can be expanded as required.

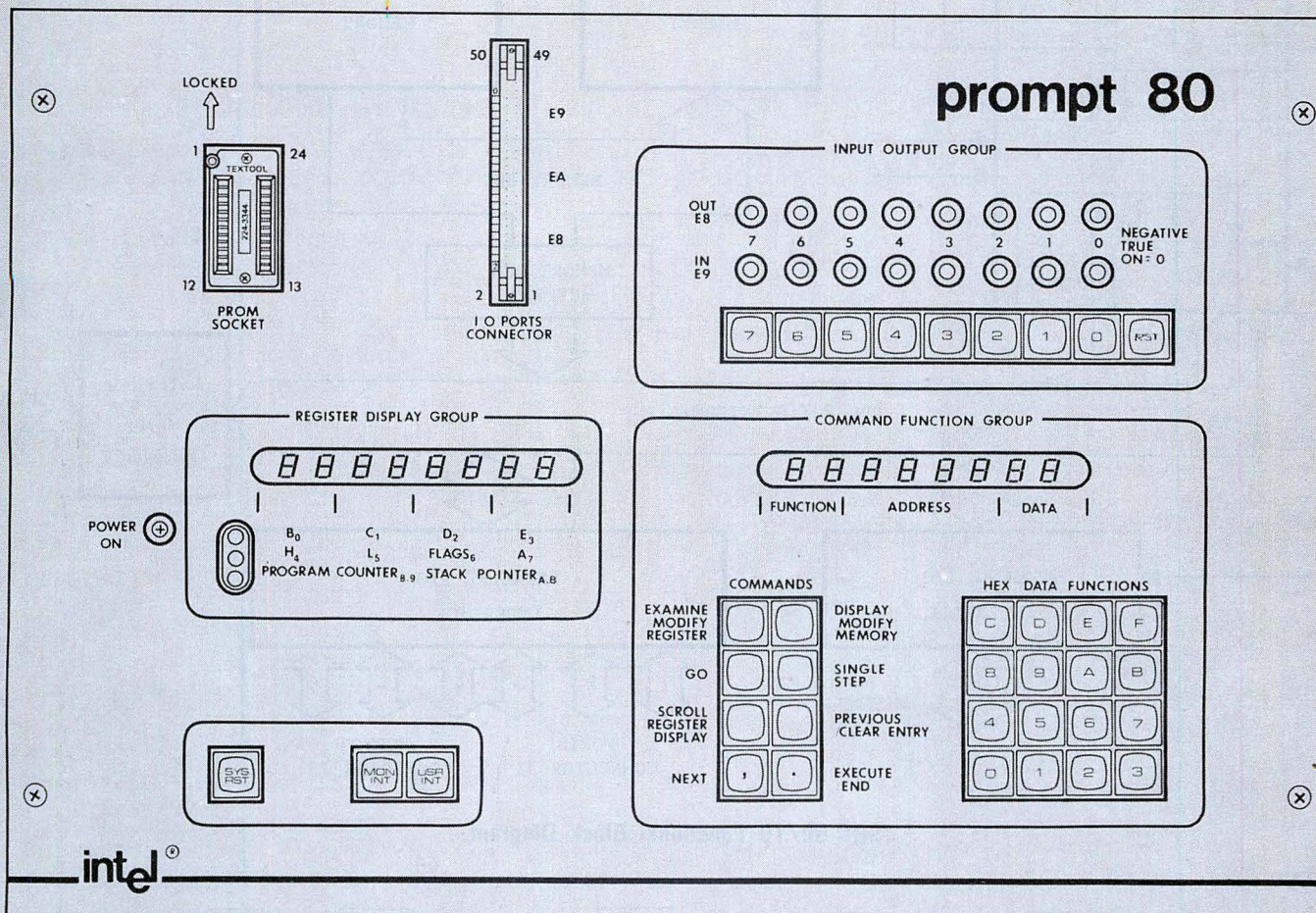


Figure 2. Panel Operation

ADDITIONAL SUPPORT

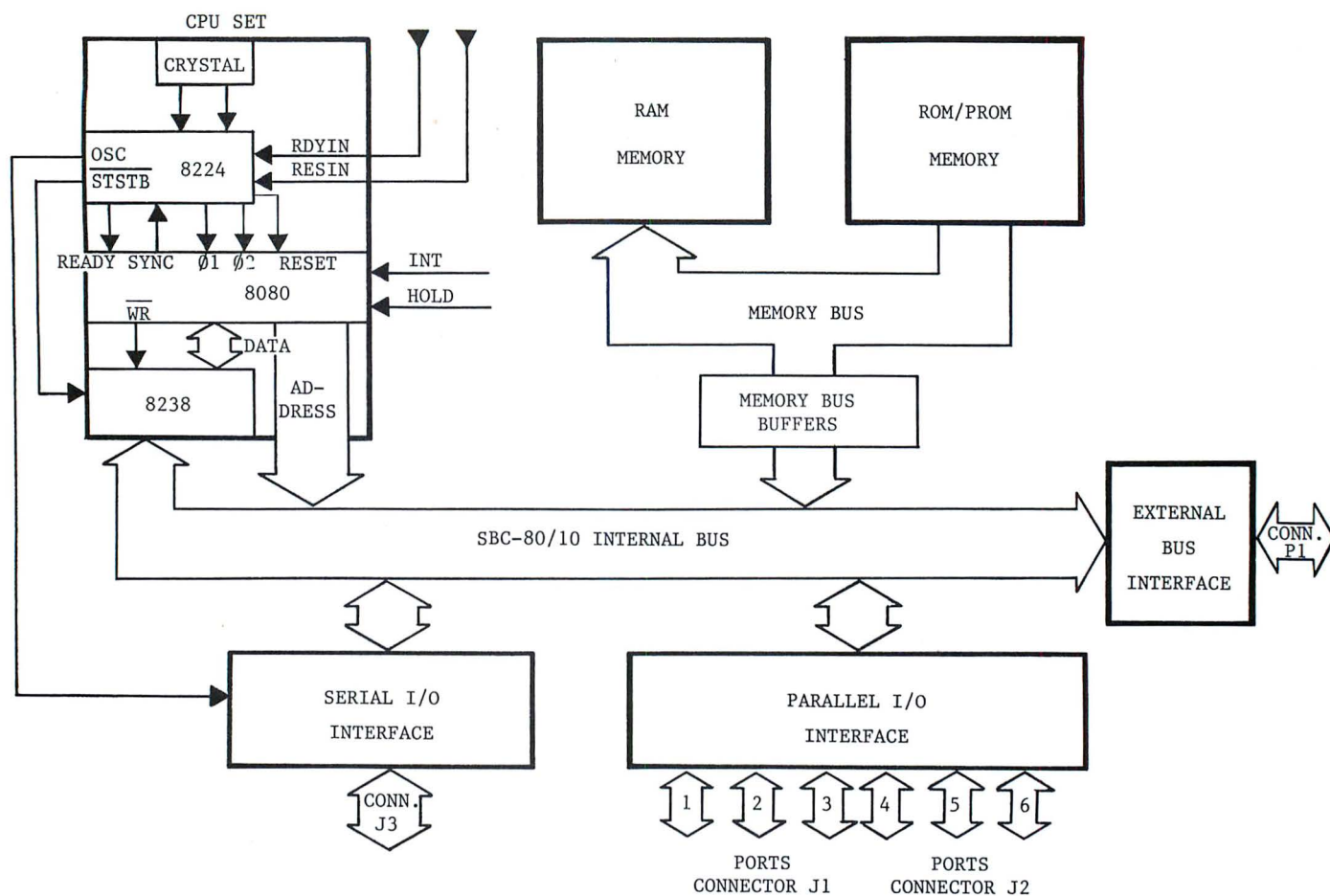
A major portion of those users who will invest in a low cost microcomputer system will have had little or no experience in microcomputing. For this reason, additional design and tutorial information is included with the PROMPT 80 System. Part of the tutorial material consists of programming examples which are stored in one of the extra EPROM's that can run on the PROMPT 80 System while illustrating its uses. In conjunction with the design library is a comprehensive tutorial manual which explains microcomputing and programming concepts with novel MICROMAP* diagrams that explain the relationships among instructions for memory, input/output and internal CPU operations. A full set of reference schematics are also included with the PROMPT 80 System.

The Intellec PROMPT 80 Personal Programming Tool is now available at \$1495. The price includes complete assembly and testing, two 8708 EPROM's, three 8308 ROM's containing the system monitor programs, along with the design library. Optional accessories include a cable for connection to the Intellec

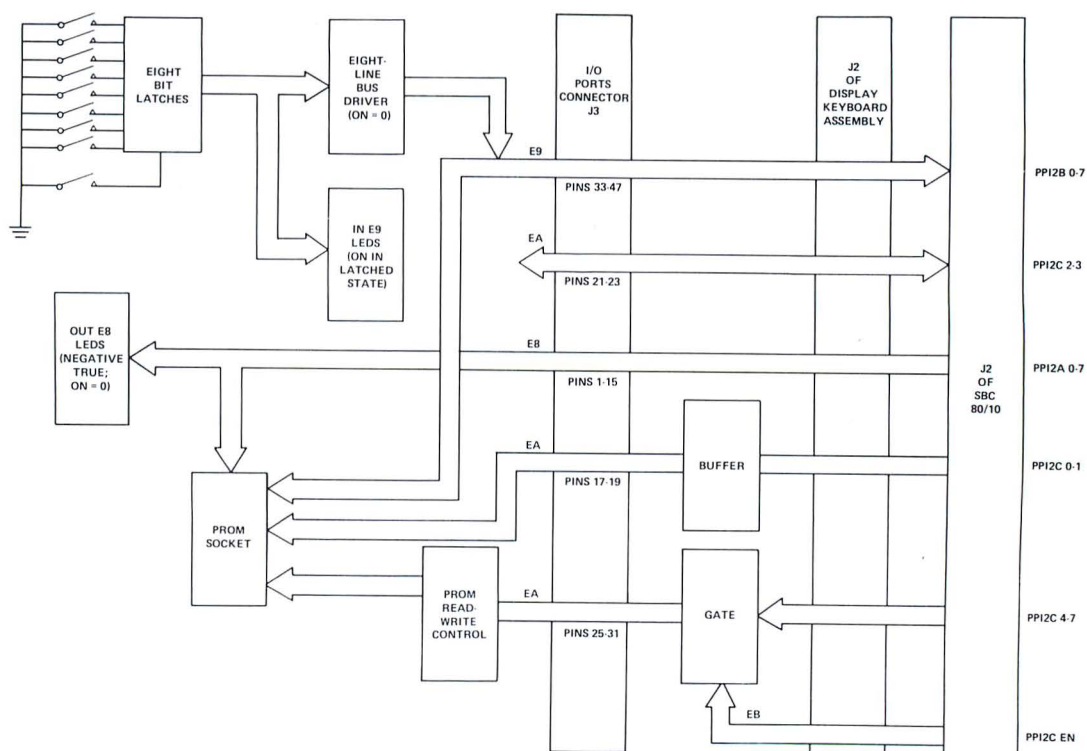
Microcomputer Development System as a specialized PROM programmer; a cable for connection to the serial port for addition of a terminal; expansion modules including memory boards, I/O boards, combination memory and I/O boards, card cage and backplane modules, a diskette controller module, and diskette systems.

In summary the PROMPT 80 System offers the beginner a means of easily learning microcomputing and provides a convenient method for debugging programs. The fact that it can be expanded both in capacity and peripheral support makes it a cost effective base for building a complete microcomputer system.

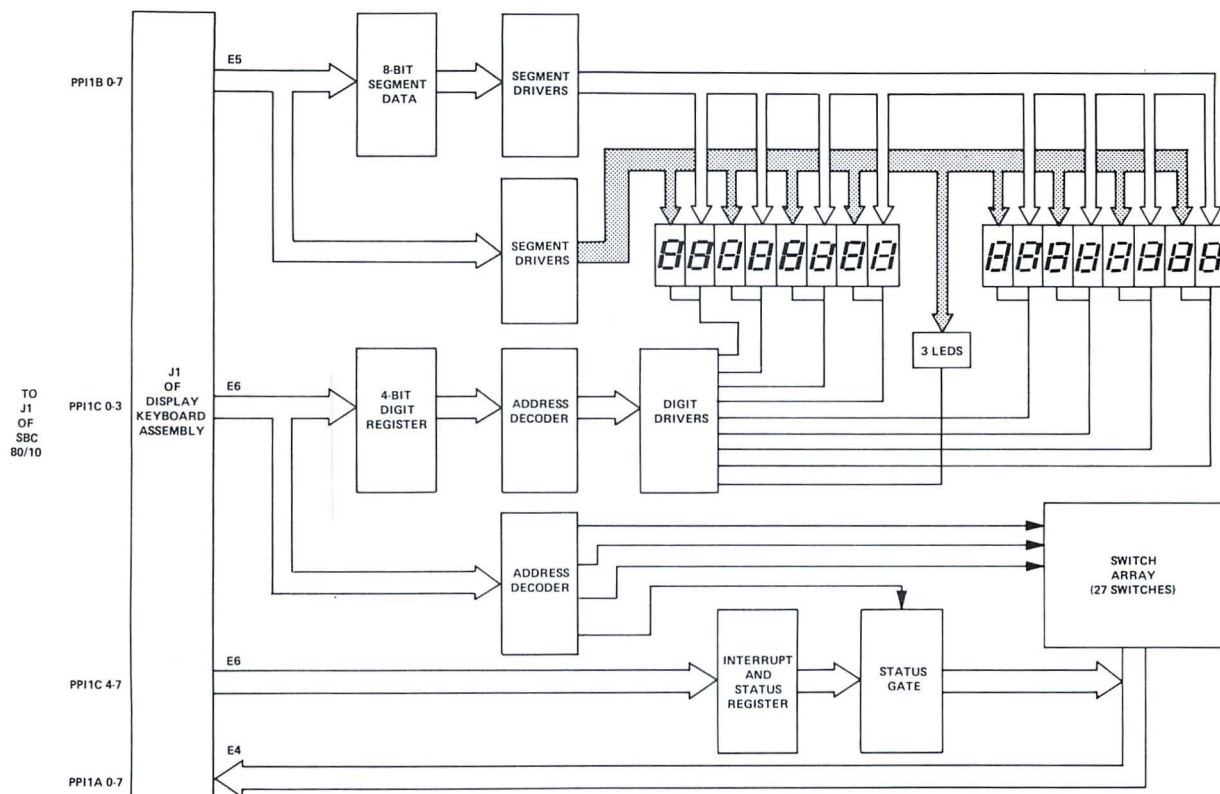
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SBC-80/10 Functional Block Diagram



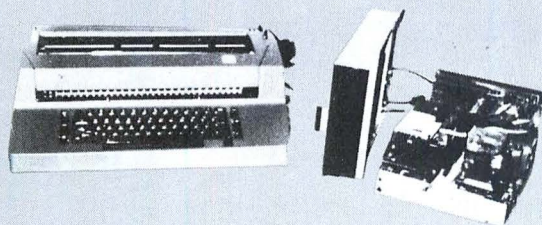
Display Keyboard Assembly, Display & Keyboard Functions, Block Diagram



Display Keyboard Assembly, I/O & PROM Programming Functions, Block Diagram

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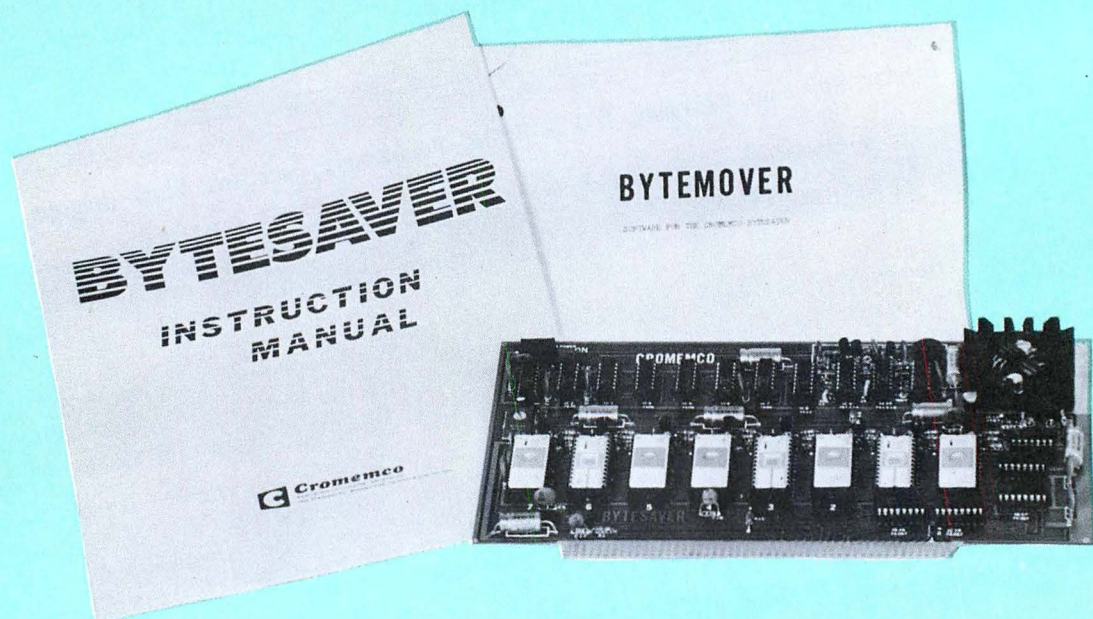
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Manuals from above kits are offered for the purpose of evaluating the kits. Refunds for manuals apply on subsequent kit order.

SK-D1	Selectric Conversion Manual	6.50
SK-D2	Selectric Programming Manual, with listings and timing data.	6.50
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CARD-OF-THE- MONTH

CROMEMCO BYTESAVER™



by Roger Edelson

Are you tired of reentering your favorite program everytime you turn off power? Does the thought of waiting 15 minutes for your BASIC to read in fill you with dread? Would you like to have your assembler/editor/monitor available within one second after turn-on? If you answered yes to any of these questions, then you ought to consider this month's card — the CROMEMCO BYTESAVER™.

If I could purchase one board (after some memory and an I/O card) the BYTESAVER would be my choice. The board is both an economical PROM (Programmable Read Only Memory), with the capacity for a full 8K bytes of storage, and a low-cost means of storing your programs in PROM. The BYTESAVER™ is an S-100 bus compatible memory board. Space is provided for eight 2708 U.V. erasable PROMs, for a full 8K bytes of memory. Using the 2708 allows your 8080 machine to operate no wait states, however, provision for a wait state is provided should you desire to purchase slower 2704 or 2708 PROMs.

The BYTESAVER™ also provides you with your own low cost PROM programmer. Using the software provided programs may be transferred from non-permanent RAM memory to the permanent PROM memory in the BYTESAVER™. Once your program is stored in PROM it's protected from power turn-offs, either accidental or intentional. The PROMs used are U.V. erasable and may be used again and again. Your program may be run either directly out of PROM, or using the software provided, it may be transferred to RAM memory beginning at any 1K segment selected. The software provided with the BYTESAVER™ controls both the transfer of data from the PROMs or to the PROMs. It is designed so there is no need for a keyboard. Just set the computer sense switches as instructed in the documentation. Transfer of RAM content to PROM takes less than a minute, and transfer of the 8K from PROM to RAM is complete in less than one second. The software controls the computer lights to provide verification of complete and accurate transfer of memory content.

As far as the design goes, the BYTESAVER™ is not particularly complex. The board is S-100 bus (ALTAIR/IMSAI) compatible, and contains space for eight 2708/2704 PROMs. In order to program the eight 2708 PROMs a high voltage (+30V) supply is required, and this is generated from the regulated +5V supply by a DC to DC Converter. Switching (Protect/-Unprotect) is provided to disable this supply to avoid inadvertent overwrite of the memory in the case of a user program malfunction. The DC to DC converter appears to be a standard blocking oscillator configuration with a very simple feedback regulator. I say appears because the schematic does not show the internal arrangement of the pulse transformer used in the converter. Since there is hardly anything magic about a blocking oscillator it seems strange that Cromemco doesn't help those of us who might be able to service our own boards by including the transformer arrangement.

Distribution of the program voltage to the 2708s is by means of discrete transistors controlled by 7406 open-collector inverting buffers. A schematic of the BYTESAVER™ is shown in Figure 3. Control of the CS/WE pin (which requires +12 V during WRITE) is done by a 7406 and a discrete transistor which allows

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this pin to float up to +12V. During READ operation the $\overline{CS}/\overline{WE}$ pin is either a ground or +5V, as the +12V supply is disabled.

While we are discussing the schematic let me suggest to Cromemco that the 7406 is an inverting buffer and I would prefer it to be shown that way, always. It is difficult to follow a logic diagram if the inverting sign is left out, even if it is desired to show logical flow. If necessary an inverting circle could have been placed at the $\overline{CS}/\overline{WE}$ input pin at the 2708. A further help would have been to have the component designation on the schematic also. These are all minor quibbles, however, and they do not detract from the board's usefulness and operation.

Returning to the BYTESAVER™ circuit, the data bus lines are all buffered by 74367's (the standard 54/74 equivalent to the ubiquitous 8T97 series). Address decoding for the highest 8K of memory (A13-A15) is provided by jumper connections on the board. In order to provide addressing in this fashion using a three input NAND gate (rather than the slightly more expensive and easier to use octal decoder and dip switch) inverted address signals must be made available. Three inverters of a 74LS04 are used to derive $\overline{A13}$, $\overline{A14}$, and $\overline{A15}$. Since there were three inverters left over, these were used to buffer the A10 through A12 signals to the 7442. For this reason the low order address selects the output 7 pin. A bit strange but it works, and very well.

A 74123 dual retriggerable one-shot is used to provide the proper pulse width (N/MS) needed for programming the PROM. This pulse is also used to produce a wait state during PROM programming. As mentioned earlier, it is possible to jumper connect the capability for one wait state if slower PROMs are used. This is done at the input to the three input NAND gate whose output drives the clear pin on the second half of the 7474 'D' type Flip-Flop.

The board is high quality G-10 material with tinned solder pads and gold plated edge board connectors for reliability. The kit is fully socketed and assembly is suggested to be about one evening; it doesn't even take that long. A high quality soldermask contributes to the ease of assembly and minimizes the chance of solder splashes. The assembly instructions are explicit enough and the board is adequately screened to provide easy identification of component placement. Cromemco recommends no diode be installed in the position below QO. This will prevent inadvertant re-write of the BYTEMOVER™ stored in PROM O. The assembly instructions also warn that a pair of IC regulators look physically similar, BUT are NOT interchangeable. Also a nylon screw is provided to prevent shorting a regulator to ground.

One of the niceties of the BYTESAVER™ is the capabilities provided by its software. When you purchase a BYTESAVER™ with one 2704 PROM, the Bytemover software is pre-programmed in that PROM. For your information and assistance, Cromemco has allowed INTERFACE AGE to publish the BYTEMOVER™ software. This program is included at the end of this article.

The PROM containing the Bytemover software is normally inserted into PROM location Zero on the Bytesaver board.

The Bytemover software can be used to program a

PROM in any of the PROM locations on the Bytesaver board. The Bytemover software can also be used to transfer programs from PROM to RAM.

The operation of the Bytemover software is controlled by setting front panel sense switches on any S-100 bus compatible computer. However, to use the Bytemover software there must be at least one RAM board in the computer beginning at location Zero in the memory map. Furthermore, this RAM board must be unprotected for proper execution of the Bytemover software.

Software can be loaded into a 2704 or a 2708 in as small increments as you desire provided it is added to previously unused areas in that PROM.

This is done by first using Bytemover to move the current contents of the PROM down to RAM which corresponds to the unused portion of the PROM and finally using Bytemover again to reprogram the PROM with the new software.

Although the entire PROM must always be programmed, it never hurts to re-write the same information over again. And, of course, an erased PROM in which all bits are "1" may be programmed at any time.

In general, it is OK to write a "1" over a "1", a "0" over a "0", or a "0" over a "1", but to write a "1" over a "0" the PROM must be completely erased.

If the PROM to which you want to add software is PROM zero on the Bytesaver board, turn off AC power to the computer and install a 1N914 diode just below QO. Turn the power back on and move Bytemover to RAM zero. Add the new software to an area of RAM which corresponds to an unused portion of PROM zero.

Re-program PROM zero by following the example in the manual supplied. Note you need not erase the PROM to do this. Turn the computer power off and remove the 1N914 diode below QO.

The Bytesaver software supplied with the board is designed to program the PROM in approximately 30 seconds. This is generally a sufficiently long period of programming time. However, to be completely within the manufacturer's specifications, the PROM should be programmed for two to three minutes.

If you wish to program your PROMs for longer than 30 seconds, the Bytemover software may be easily modified. Simply change the contents of memory location 77H (Hex) from 40H to 00H. Now you must manually time the programming operation and depress the stop switch at the end of the operation.

Before using the Bytesaver, you must install three jumper wires to set the location of the Bytesaver in memory. This adjustment is shown in Figure 1. The assembled Bytesaver comes with A13, A14, and A15 each tied to the corresponding 'H1' pad to position the board at the very top of memory. In the following instructions it is assumed this is the jumper connection used.

1. Turn off all power to the computer and plug in the Bytesaver board.
2. Be sure the program power on the Bytesaver is turned off (program power switch in the down position).
3. Turn on the computer. Raise the reset switch, the stop switch and then raise the reset switch once again to initialize the computer.

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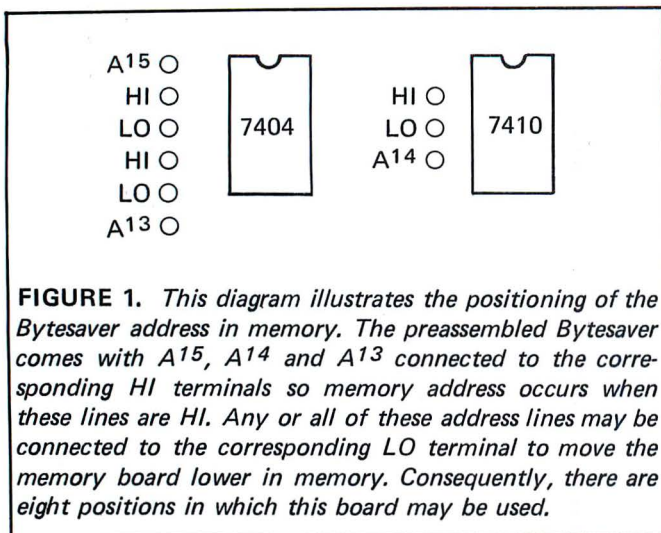
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4. Raise the address switches A¹⁵, A¹⁴, and A¹³. All other address switches should be in the down position.
5. Raise the examine switch. You are now examining the contents of the first byte of PROM in PROM location zero of the Bytesaver memory board (memory location 340 000). If the PROM supplied with your Bytesaver is in this PROM location, the data lights will read '061', the first byte of the Bytemover program.

The following examples show the steps needed to transfer and program the PROMs and the ease in which it is done.

EXAMPLE 1: Transfer the Bytemover Program from PROM to RAM beginning at RAM location Zero.

1. Raise the reset switch.
2. Depress the unprotect switch (on the Altair front panel).
3. Raise A¹⁵, A¹⁴, and A¹³. Raise the examine switch. The data lights should read '061' octal.
4. Now set the sense switches for the task to be done, referring to Figure 2.
5. Push the run switch. In less than one second, the contents of PROM will be transferred to RAM. The contents of PROM are unaffected by this operation.
6. Raise the stop switch.
7. Raise the reset switch. Note that the data lights read '061.'

EXAMPLE 2: Program a 2708 PROM inserted in PROM location one. This PROM is to be programmed with the contents of the first 1K bytes of RAM beginning at location zero in memory. The Bytesaver software is still in the PROM installed in PROM location zero on the Bytesaver board.

A ¹⁵	Down	to transfer from Prom to Ram.
A ¹⁴	Down	for the transfer of 1K bytes.
A ¹³	Down	All down since we are transferring from the PROM that contains Bytemover (PROM 0).
A ¹²	Down	
A ¹¹	Down	
A ¹⁰	Down	All down for storage to begin at location zero in RAM.
A ⁹	Down	
A ⁸	Down	

1. Raise the reset switch.
2. Depress the unprotect switch on the Altair front panel).
3. Raise A¹⁵, A¹⁴, and A¹³. Raise the examine switch. The data lights should read '061' octal.
4. Raise the protect switch on the Bytesaver board (i.e. program power switch to the on position). The protect light on the front panel should turn off when this switch is raised.
5. Now set the sense switches for the task to be done.

A ¹⁵	Up	to program a PROM
A ¹⁴	Down	(always down for PROM programming).
A ¹³	Down	To select the PROM 1K higher in memory than the PROM that contains Bytemover
A ¹²	Down	
A ¹¹	Up	
A ¹⁰	Down	All down for transfer to begin at location zero in RAM.
A ⁹	Down	
A ⁸	Down	

6. Push the run switch. Note that panel light A⁹ is blinking at a rate of about twice per second. When this light stops blinking, the PROM programming is complete.









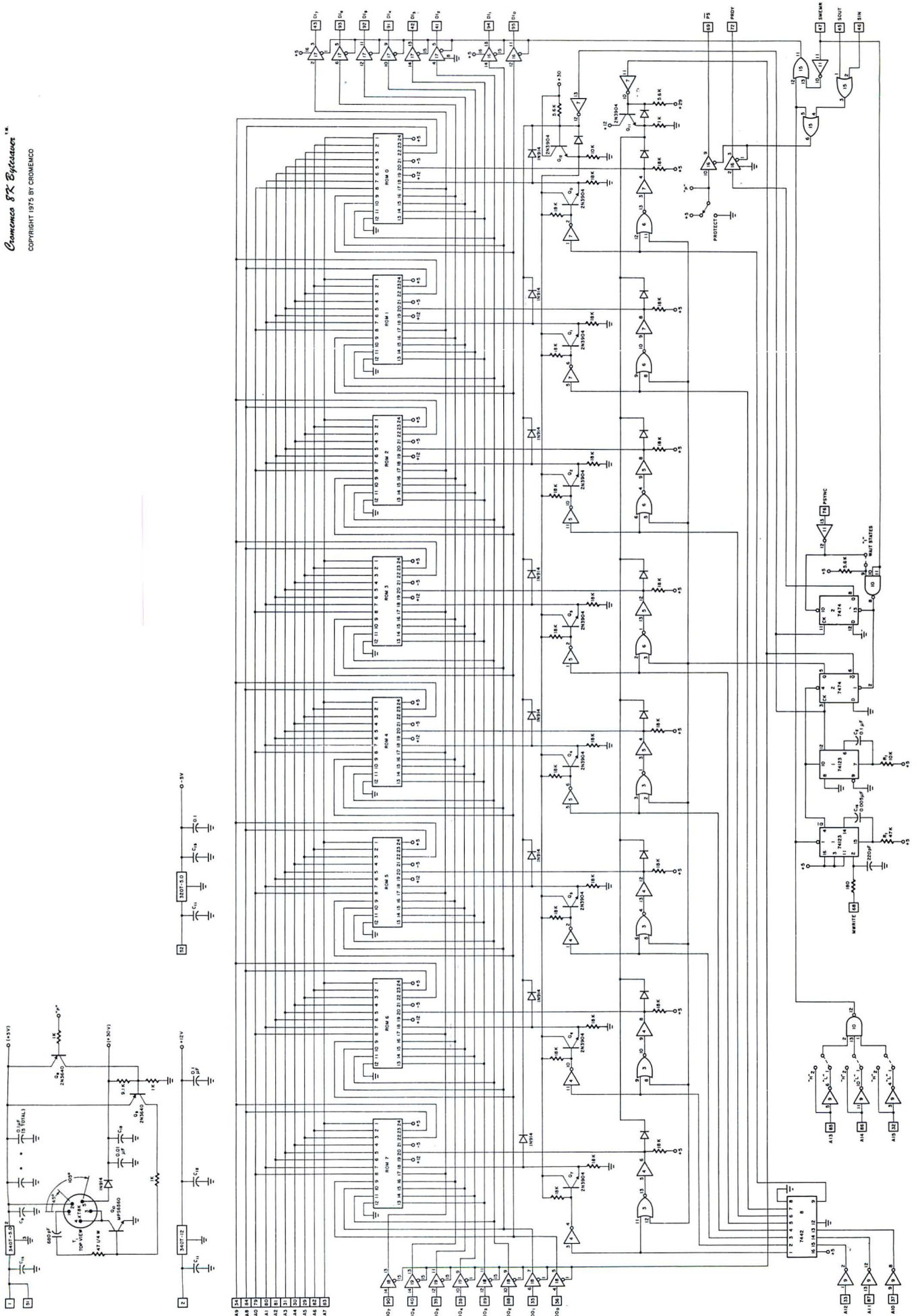
A ¹⁵	A ¹⁴	A ¹³	A ¹²	A ¹¹	A ¹⁰	A ⁹	A ⁸
							
Up To program a PROM.	Up For a 7K transfer.	MSB		LSB	MSB		LSB
Down To move from PROM to RAM.	Down For a 1K transfer.	PROM address location in increments of 1K from the PROM in which BYTE			Selection of RAM address in 1K increments.		

FIGURE 2. FUNCTION OF THE SENSE SWITCHES IN BYTEMOVER.



7. Raise the stop switch.
8. Now note the INTE light on the front panel. If this light is on, the Bytemover Verifier has verified that the contents of the programmed PROM are indeed identical to the contents of the selected 1K bytes of RAM. If this light is off, the PROM is not programmed correctly. This could be due to a defective PROM.

EXAMPLE 3: Altair 8K BASIC can be stored in seven 2708 PROMs. Given that these seven PROMs are in PROM locations one through seven of the Bytesaver board, 8K BASIC can easily be transferred into RAM using the following procedure.

1. Raise the reset switch.
2. Depress the unprotect switch (on the Altair front panel).
3. Raise A₁₅, A₁₄, and A₁₃. Raise the examine switch. The data lights should read '061' octal.
4. Now set the sense switches for the task to be done.

A15	Down	to transfer from PROM to RAM.
A14	Up	
A13	Down	for a 7K transfer.
A12	Down	
A11	Up	To begin transfer from the PROM 1K higher in memory than the Bytemover program.
A10	Down	
A9	Down	All down for storage to begin at location zero in RAM.
A8	Down	

5. Push the run switch. In less than one second BASIC will be loaded into RAM (it sure beats paper tape!). Now raise the stop switch.

EXAMPLE 4: If you do not have Bytemover in PROM, you can program a PROM with Bytemover that is stored in RAM. The Bytemover software must be loaded into RAM beginning at location zero. The Bytemover software can then be burned into a PROM using the following procedure.

1. Raise the reset switch.
2. Depress the unprotect switch (on the Altair front panel).
3. Insert an erased PROM into PROM location zero.
4. Examine location 000 240 in memory.
5. Raise the program power switch on the Bytesaver board.
6. Set the sense switches with A₁₅, A₁₄, and A₁₃ up.
7. Push the run switch. When the A₉ light stops blinking, the programming is complete. The INTE light will be on.
8. Turn off PROM program power by depressing the switch on the Bytesaver board.

That's about all there is to it to use a Bytesaver. It's both convenient and easy. The new instruction manual is a great improvement over the previous one. I would have liked to have a little more information on erasing PROMs. The PROM should be about one inch away

and exposed for about twenty minutes. This assumes an integrated dosage of 10W-SECS/CM² is required. If shorter times or lower output devices are used, I would recommend placing the PROMs in the Bytesaver and running a memory check. All bits should be '1' for correct operation. PROM erasers are available from various computer stores around the country.

The Bytesaver is a tremendous adjunct to your computer capability (I have two, one with an assembler/monitor program and the other with BASIC residing in memory). If you expect to program a greater number of different PROMs you would be wise to replace the PROM sockets with low or zero insertion force types. Either that or place the PROM in carriers. This is to reduce the strain on their leads. The Bytesaver may be purchased with the Bytemover software already stored in either a 2704 or a 2708. By the way, the 2704 is just a 2708 with a bad bit in the upper 512 bytes. 2708 PROMs can also be purchased from Cromemco, but their price is a little higher than you can get elsewhere, but the convenience may be worthwhile. Anyway if you choose to buy it, I would heartily recommend considering the Cromemco Bytesaver as your next purchase.

```

0000      0000 * BYTEMOVER (T.M.) SOFTWARE FOR
0000      0001 * CROMEMCO 8K BYTESAVER (T.M.)
0000      0002 * VERSION 3. 1
0000      0003 * SELF-RELOCATING SOFTWARE LOCATABLE AT ANY
0000      0004 * 1024 BYTE (1K) BOUNDARY IN MEMORY
0000      0009 * ROUTINE TO FIND ONESELF IN MEMORY
0000      0010 SP EQU 6
0000      0019 * DEFINE FIRST 4 BYTES IN MEMORY AS STACK
0000 31 00 00 0020 LXI SP, 0
0003      0029 * SAVE FIRST FOUR BYTES IN REGISTERS
0003 C1      0030 POP B
0004 D1      0040 POP D
0005      0049 * REPLACE BYTE 0 WITH A 'RETURN'
0005 2E C9      0050 MVI L, 0C9H
0007 F3      0051 DI
0008 E5      0060 PUSH H
0009 E5      0070 PUSH H
000A 00      0080 NOP
000B 00      0081 NOP
000C 00      0082 NOP
000D 31 04 00 0090 LXI SP, 4
0010 CD 00 00 0100 CALL 0
0013      0101 * ROM LOCATION NOW IN BYTE 3
0013 31 02 00 0110 LXI SP, 2
0016 E1      0120 POP H
0017      0129 * RETURN BYTES 0-3
0017 31 04 00 0130 LXI SP, 4
001A D5      0140 PUSH D
001B C5      0150 PUSH B
001C      0159 * STORE ROM LOCATION IN SP
001C F9      0160 SPHL
001D 0E 00      0170 MVI C, 0
001F 59      0180 MOV E, C
0020 69      0190 MOV L, C
0021      0199 * INPUT SENSE SW COMMANDS
0021 DB FF      0200 IN 255
0023 57      0210 MOV D, A
0024      0219 * STRIP RAM ADDRESS
0024 E6 07      0220 ANI 7
0026 07      0230 RLC
0027 07      0240 RLC
0028      0249 * STORE RAM ADDRESS IN BC
0028 47      0250 MOV B, A
0029 7A      0260 MOV A, D
002A      0269 * STRIP ROM ADDRESS
002A E6 38      0270 ANI 56
002C 0F      0280 RRC
002D 00      0290 NOP
002E 67      0300 MOV H, A
002F 39      0310 DAD SP
0030 2E 00      0320 MVI L, 0
0032 7A      0330 MOV A, D
0033 EB      0340 XCHG
0034      0341 * ADDRESS OF ROM BEING PROCESSED IN DE
0034      0349 * BRANCH TO TRANSFER OR PROGRAM ROUTINE

```


0034 E6 80	0350 ANI 128	0063 60	1040 MOV H, B
0036 0F	0360 RRC	0064	1049 * MOVE RAM ADDRESS INTO SP
0037 0F	0370 RRC	0064 F9	1050 SPHL
0038 C6 2D	0380 ADI 45	0065 67	1060 MOV H, A
003A 21 00 00	0390 LXI H, 0	0066 2E 6B	1070 MVI L, 107
003D 6F	0400 MOV L, A	0068	1079 * INCREMENT RAM ADDRESS
003E 39	0410 DAD SP	0068 01 00 00	1080 LXI B, 0
003F E9	0420 PCHL	006B	1089 * INCREMENT RAM ADDRESS
0040	0500 * ROUTINE TO TRANSFER ROM TO RAM	006B 3B	1090 DCX SP
0040 F9	0510 SPHL	006C	1098 * USE STAX AND POP 6 (PSW)
0041 21 0B 00	0520 LXI H, 11	006C	1099 * TO MOVE DATA FROM ROM TO RAM
0044 39	0530 DAD SP	006C F1	1100 POP 6
0045 EB	0550 XCHG	006D 12	1110 STAX D
0046 F9	0560 SPHL STACK CONTAINS ROM LOCATION	006E	1119 * INCREMENT ROM ADDRESS
0047 EB	0570 XCHG H&L CONTAIN LOOP ADDRESS	006E 13	1120 INX D
0048 11 00 00	0580 LXI D, 0	006F	1129 * INCREMENT BYTE COUNT
0048	0588 * START OF TRANSFER LOOP	006F 03	1130 INX B
0048	0589 * INCREMENT ROM ADDRESS	0070	1138 * B STORES TWO CONSTANTS
0048 3B	0590 DCX SP	0070	1139 * # COMPLETE PASSES & IN ROM CNT
004C	0599 * MOVE DATA FROM ROM TO RAM	0070 78	1140 MOV A, B
004C F1	0600 POP 6	0071	1149 * # PASSES = 32 ?
004D 02	0610 STAX B	0071 FE FC	1150 CPI 252
004E	0619 * INCREMENT RAM ADDRESS	0073 3F	1160 CMC
004E 03	0620 INX B	0074 1F	1170 RAR
004F	0629 * INCREMENT BYTE COUNT	0075 1F	1180 RAR
004F 13	0630 INX D	0076	1198 * SET 64 TO 0 FOR TWO MINUTE TIMER VERSION
0050 7A	0640 MOV A, D	0076 E6 40	1200 ANI 64
0051 E6 04	0650 ANI 4	0078	1201 * A=64 IF COMPLETED 32 PASSES
0053 07	0660 RLC	0078 2E 7D	1205 MVI L, 7DH
0054 07	0670 RLC	007A 85	1210 ADD L
0055 00	0680 NOP	007B 6F	1220 MOV L, A
0056 85	0690 ADD L	007C E9	1225 PCHL
0057 6F	0070 MOV L, A	007D 2E 6B	1226 MVI L, 6BH
0058 E9	0710 PCHL	007F 78	1230 MOV A, B
0059 00	0716 NOP	0080 E6 04	1240 ANI 4
005A 00	0717 NOP	0082	1241 * A=4 IF END OF 1024 BYTE PASS
005B	0719 * JUMP TO 00B1 FROM TRANSFER ROUTINE	0082 07	1250 RLC
005B 3E 56	0720 MVI A, 56H	0083 07	1260 RLC
005D 85	0725 ADD L	0084 07	1270 RLC
005E 6F	0730 MOV L, A	0085 85	1280 ADD L
005F E9	0740 PCHL	0086 6F	1290 MOV L, A
0060	1000 * ROUTINE TO PROGRAM ROM	0087	1291 * GO BACK TO 1090 UNLESS OVERFLOW
0060 00	1010 NOP	0087	1292 * THEN GO TO 1380 FOR
0061	1019 * MOVE RAM ADDRESS INTO HL	0087	1293 * ADDRESS SUBTRACTION
0061 69	1020 MOV L, C	0087	1294 * OR 2135 FOR QUIT
0062 7C	1030 MOV A, H	0087 E9	1300 PCHL

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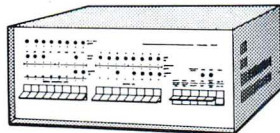


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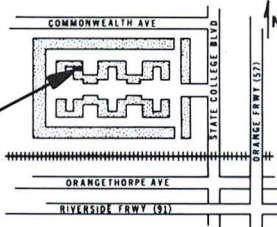
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CIRCLE INQUIRY NO. 40

0088 00	1350 NOP
0089 00	1360 NOP
008A 00	1370 NOP
008B	1378 * ANOTHER PROGRAM PASS TO BE DONE
008B	1379 * ADJUST ROM AND RAM ADDRESSES
008B 7C	1380 MOV A, H
008C 21 00 FC	1390 LXI H, 64512
008F	1399 * SUBTRACT 1024 FROM ROM ADDRESS
008F 39	1400 DAD SP
0090 F9	1410 SPHL
0091 21 00 FC	1420 LXI H, 64512
0094	1429 * SUBTRACT 1024 FROM RAM ADDRESS
0094 19	1430 DAD D
0095 EB	1440 XCHG
0096 67	1450 MOV H, A
0097 2E 6B	1460 MVI L, 107
0099 78	1470 MOV A, B
009A E6 F8	1480 ANI 248
009C	1489 * INCREMENT PASS COUNTER BY ONE
009C C6 08	1490 ADI 8
009E 47	1495 MOV B, A
009F	1499 * GO BACK TO 1090
009F E9	1500 PCHL
00A0	2000 * ROUTINE TO LOAD BYTEMOVER INTO ROM
00A0 DB FF	2010 IN 255
00A2 47	2020 MOV B, A
00A3 E6 E0	2030 ANI 224
00A5 1E 00	2040 MVI E, 0
00A7 4B	2050 MOV C, E
00A8 57	2060 MOV D, A
00A9 78	2070 MOV A, B
00AA E6 1F	2080 ANI 31
00AC 47	2090 MOV B, A
00AD 67	2100 MOV H, A
00AE 2E 60	2110 MVI L, 96
00B0 E9	2120 PCHL
00B1	2121 * CHECK FOR 7K TRANSFER OF ROM TO RAM
00B1 C6 1A	2122 ADI 1AH
00B3 6F	2123 MOV L, A
00B4 DB FF	2124 IN 255
00B6 E6 40	2125 ANI 64
00B8 0F	2126 RRC
00B9 0F	2127 RRC
00BA 85	2128 ADD L
00BB 6F	2129 MOV L, A
00BC E9	2130 PCHL
00BD	2133 * PROGRAMMER VERIFICATION ROUTINE
00BD	2134 * PART 1
00BD 7C	2135 MOV A, H
00BE 21 00 FC	2145 LXI H, 64512
00C1 39	2155 DAD SP
00C2 F9	2165 SPHL
00C3 2E CD	2175 MVI L, 0CDH
00C5 67	2185 MOV H, A
00C6 E9	2195 PCHL
00C7 00	2205 NOP
00C8 00	2210 NOP
00C9 00	2215 NOP
00CA 00	2220 NOP
00CB	2229 * ROM TO RAM TRANSFER STOP ROUTINE
00CB FB	2230 EI
00CC E9	2240 PCHL
00CD	2248 * PROGRAMMER VERIFICATION ROUTINE
00CD	2249 * PART 2
00CD 7C	2250 MOV A, H
00CE 21 00 FC	2260 LXI H, 64512
00D1 19	2270 DAD D
00D2 EB	2280 XCHG
00D3 2E F1	2290 MVI L, 0F1H
00D5 67	2300 MOV H, A
00D6 01 00 00	2310 LXI B, 0
00D9 E9	2320 PCHL
00DA 00	2625 NOP
00DB	2629 * 7K TRANSFER COMPLETION CHECK
00DB D6 90	2630 SUI 90H
00DD 6F	2640 MOV L, A
00DE 7A	2650 MOV A, D
00DF C6 04	2660 ADI 4
00E1 57	2670 MOV D, A
00E2 FE 38	2680 CPI 56
00E4 3F	2685 CMC
00E5 3E 00	2690 MVI A, 0
00E7 1F	2700 RAR
00E8 85	2710 ADD L
00E9 6F	2720 MOV L, A
00EA E9	2730 PCHL
00EB	2879 * ROM PROGRAMMER STOP ROUTINE
00EB 00	2880 NOP
00EC 00	2881 NOP
00ED FB	2885 EI
00EE E9	2890 PCHL
00EF E9	2900 PCHL

00F0 E9	2906 PCHL	0101 EB	3058 XCHG
00F1	2918 * PROGRAMMER VERIFICATION ROUTINE	0102 86	3059 ADD M
00F1	2919 * PART 3	0103 EB	3060 XCHG
00F1 3B	2920 DCX SP	0104 C6 07	3061 ADI A, 1
00F2 F1	2930 POP 6	0106 3F	3065 CMC
00F3 EB	2940 XCHG	0107 17	3070 RAL
00F4	2949 * COMPARE FOR GREATER	0108 E6 01	3090 ANI 1
00F4 BE	2950 CMP M	010A 2F	3100 CMA
00F5 EB	2960 XCHG	010B 3C	3101 INR A
00F6 17	2970 RAL	010C 85	3105 ADD L
00F7 E6 01	3000 ANI 1	010D 6F	3110 MOV L, A
00F9 2F	3010 CMA	010E 03	3130 INX B
00FA 3C	3011 INR A	010F 13	3140 INX D
00FB 85	3015 ADD L	0110 78	3150 MOV A, B
00FC 6F	3020 MOV L, A	0111 E6 04	3180 ANI 4
00FD 3B	3030 DCX SP	0113 2F	3190 CMA
00FE 3B	3040 DCX SP	0114 3C	3191 INR A
00FF	3050 * COMPARE FOR LESSER	0115 85	3195 ADD L
00FF F1	3055 POP 6	0116 6F	3200 MOV L, A
0100 2F	3056 CMA	0117 E9	3210 PCHL

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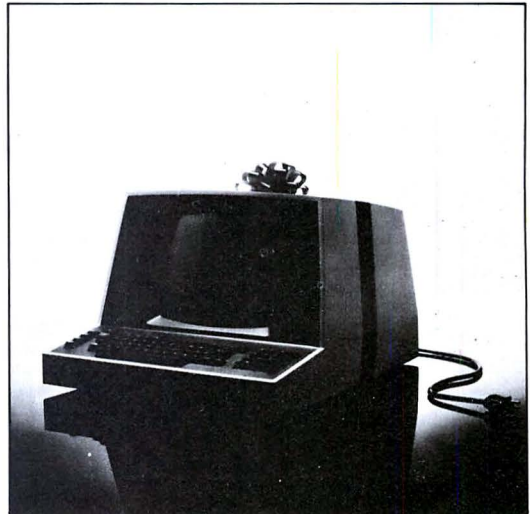
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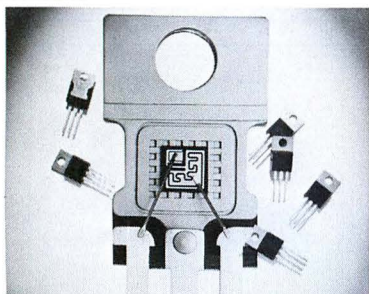
CIRCLE INQUIRY NO. 49

New Products

COMPONENTS

Motorola to "Alternate-Source" Popular Plastic Power Transistors

Motorola has supplemented its extensive line of plastic-packaged power transistors with a series of 20 new devices that duplicate the more popular TI and RCA-registered devices. Included in the new offering by Motorola are six Darling-ton devices and 14 discrete transistors in the 65 Watt power category. These devices are being introduced at prices that are 5 to 10 percent below published competitive prices at the time of introduction.



The introductions represent Motorola's first use of the TO-220 plastic package for silicon power transistors. This is in addition to the plastic cases, 77, 90 and 199 which have housed the company's plastic power line up to now. Customers however can continue to purchase devices with similar electrical specifications in the other Motorola plastic packages.

Motorola plans to extend its use of the TO-220 package to other power device types as quickly as production capability permits.

Product availability is now, from the factory and from authorized Motorola distributors.

For further information contact Silicon Power Marketing at (602) 244-4284 or the Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20294, Phoenix, AZ 85036.

CIRCLE INQUIRY NO. 90

8,192-Bit UV Light Erasable Programmable Read-Only Memory

The TMS 2708JL is pin-for-pin compatible with the Intel device with the same part number.



Maximum access and minimum cycle times are 450 nanoseconds. The 184 x 124 mil chip is more than 11 percent smaller than the Intel chip, potentially allowing improved manufacturing

productivity.

This smaller chip size is due to TI's unique periphery circuit design techniques which also reduce power consumed by the TMS 2708. Typical power dissipation is less than 450 milliwatts.

The memory circuit is organized as 1,024 words of 8-bit length. It is designed for high-density, fixed-memory applications where fast turnarounds and/or program changes are required.

The device is fabricated using an N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs can be driven by Series 74 TTL circuit without external resistors.

The data outputs are three-state for OR-tying multiple devices on a common bus. A pin-compatible mask programmed ROM, the TMS4700, is available for large volume systems.

The EPROM can be erased by exposing the chip through the transparent lid to high-intensity ultraviolet light at a recommended exposure of 10-watts-seconds per square centimeter.

The TMS2708 is supplied in 24-pin dual-inline ceramic packages designed for insertion in mounting-hole rows on 600-mil centers and operates from 0°C to 70°C.

Prices for each part are as follows: 1-24, \$98.00; 25-99, \$73.00; 100+, \$64.00. Parts are available now.

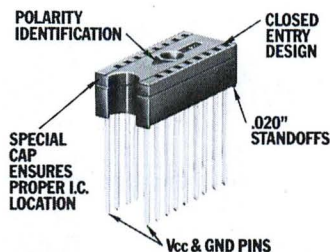
For further information contact Texas Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TMS 2708), Dallas, TX 75222; (713) 494-5115, Ext. 3281.

CIRCLE INQUIRY NO. 91

16-Pin Discrete Wrap Sockets

A unique 16-pin discrete arrangement saves labor, time, and machine costs by eliminating the need for mounting separate power and ground pins into the board. The new socket contains two additional dummy pins for commitment to Vcc and GND, and also has a specially designed cap that ensures proper insertion and location of 16-pin DIP devices.

Depending on how a particular I.C. socket board is configured, many significant savings can be realized through use of the 16-Pin Discrete. The socket need only be plugged into the board as the power and ground pins are provided as part of the socket unit. A patent has been applied for on the design of the Discrete socket.



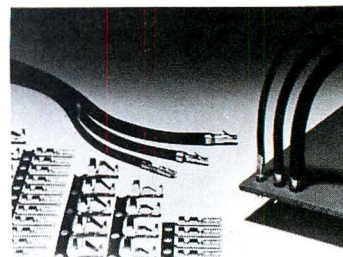
The 16-Pin Discrete has proven so successful in cost savings that Scanbe itself has taken advantage of the new concept by introducing several new 16-pin socket cards and panels, and is passing the savings gained by using the new sockets on to its customers. Typical pricing of the sockets is 39 cents each in lots of 1000.

For further information contact Scanbe Marketing Services, a Division of Zero Mfg. Co., 3445 Fletcher Avenue, El Monte, CA 91731; (213) 579-2300.

CIRCLE INQUIRY NO. 92

Strain Relief Terminal

The 4811 series terminals are used to secure wire leads to a printed circuit board prior to soldering.



Strain relief terminal eliminates leads falling out of the printed circuit board holes during component insertion and handling prior to soldering. The terminal construction allows the actual wire lead to be soldered, and because the terminal fills the printed circuit board hole, solder voiding is minimized. Due to the low insertion force, wires with crimped 4811 series terminals can be inserted into the printed circuit boards at any time during assembly and prior to soldering, without causing adjacent components to "pop" out of the printed circuit board due to excess board deflection. After soldering, the insulation crimp creates an effective strain relief eliminating the need for pre-affixed eyelets or griplets on the printed circuit board.

For further information contact Al Maag, Molex Incorporated, 2222 Wellington Court, Lisle, IL 60532; (312) 969-4550.

CIRCLE INQUIRY NO. 93

Single-Chip Microprocessor Controller

The MC10801 Microprogram Control Function is a bipolar LSI circuit, a member of the M10800 MECL Processor Family which controls the sequence of the microprogram instructions stored in a processor's control memory. The MC10801 responds to a set of 16 powerful jump and branch instructions. Mnemonic labels for each of the instructions simplify microprogram development by expressing program flow in easy-to-use assembly level language format. While designed for the M10800 Processor Family, the MC10801 is also useful as the microprogram controller in a MECL 10,000 system.

Five 4-bit I/O ports are available on the chip to shuttle control memory address information. Eight 4-bit master-slave registers in the MC10801 hold the current microprogram address, cycle as an index counter for repeats, store op-codes and flag conditions, and nest sub-routines in a 4 x 4 push/pop LIFO stack. The MC10801 also contains a "next address" logic section, which, in conjunction with the 16 jump and branch instructions, determines the information, for the next control memory address. Additional internal gates and multiplexers transfer data to and from the registers; three pins on the package convey processor status to the MC10801 for branch decisions. While organized as a 4-bit slice, MC10801s can be connected in parallel to accommodate larger control memory word length.

Compatible with all MECL 10,000 circuits, the MC10801 requires -5.2V and -2V supplies, operates over the temperature range -30°C to +85°C and is housed in a 48-pin Quil* (quad-inline) package. The price is \$50.00 in 100-999 quantities.

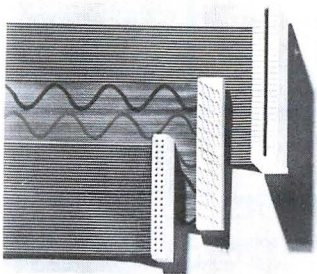
For further information contact Bi-Polar Marketing at (602) 962-2151 or the Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20294, Phoenix, AZ 85036.

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CIRCLE INQUIRY NO. 94

More Great Jumper Socket Connectors

A faster, easier and less expensive way of implementing standard double-row socket-conductor-terminated flat cable systems is an extraordinary family of Great Jumper™ Socket Connectors.



Like all Great Jumpers, these are fully pre-assembled and fully pre-tested flat ribbon cable/connector assemblies. They are available in a wide variety of configurations including several line widths, a choice of conductors, and a selection of opposite end terminations.

Particular to the Great Jumper family is an especially useful doubly-encoded Rainbow cable. This cable is color coded line-by-line on the front, and color-striped in groups of ten on the reverse. This Rainbow cable is intended for use with single-ended Great Jumpers.

The standard cable color in the Great Jumpers family is a distinctive Electric Pink.

Double-ended and daisy-chained (Great Daisy Jumpers) configurations can include not only socket connectors, but solderable printed circuit board connectors and card-edge connectors as well.

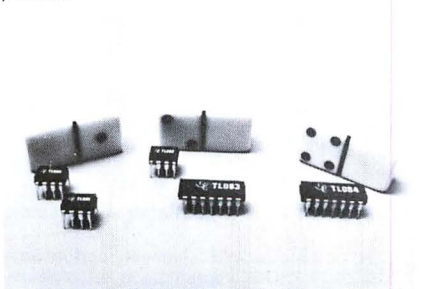
The Great Jumpers Socket Connectors use double rows of contact sockets on .100" centers. Like all great Jumpers connectors, they are molded on during factory assembly and include integral strain relief and line-by-line probeability.

For further information contact A P Products Representatives, who can be located through A P's toll-free Faster and Easier Line, (800) 321-9668.

CIRCLE INQUIRY NO. 95

Full Line of BIFET OP Amps

A full line of five BIFET operational amplifiers, including single, dual and quad circuit types, is available now from Texas Instruments Incorporated.



The op amps incorporate well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature high slew rate, low input bias and offset currents, offset voltage selection and a low offset temperature coefficient.

The single type circuits, TL080 and TL081, have offset voltage null capability and the latter requires no frequency compensation. The dual circuits, TL082 and TL083, both include internal frequency compensation. The TL083 also has offset voltage null capability. All four devices complement the previously announced TL084 quadruple op amp.

The TL080, TL081 and TL082 are offered in 8-pin plastic DIP and TO99 metal can packages. The TL083 and TL084 are available in 14-pin plastic DIP.

Prices for each part in 100-piece plastic packages for the commercial temperature range (0° to 70°C) are as follows: TL080CP, \$1.04; TL081CP, \$.52; TL082CP, \$.91; TL083CN, \$1.17; TL084CN, \$1.30. All devices are available now through TI distributors.

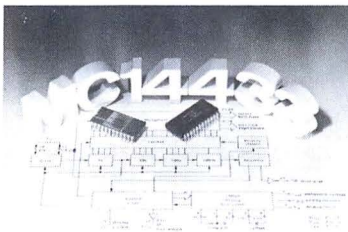
For further information contact Texas

Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: BIFET OP AMPS), Dallas, TX 75222.

CIRCLE INQUIRY NO. 96

Low Cost 3½ Digit CMOS A to D Circuit

A new single-chip CMOS integrated Circuit that requires only two external resistors and two capacitors and a single voltage reference to form a modified, dual-slope, analog-to-digital converter is now available from Motorola. It is designed for DVM/DMM, digital thermometer, digital scale applications, and can be used in MPU systems. The 3½ digit circuit, designated the MC14433, has a multiplexed BCD output format and has an intrinsic full scale range of ± 199.9 mV (200 mV reference) or ± 1.999 V (2 V reference), with an input impedance of more than 1000 megohms. The MC14433 dissipates very little power, typically 8 mW for ± 5 volt supplies. This unit operates well with both LED and LCD displays.



Other features include: $\pm 0.05\%$ of reading accuracy; Up to 25 conversions per second; Autopolarity; Auto Zero; Standard B-Series outputs; On-chip or external clock; Overrange and under-range signals. The MC14433 uses the techniques developed by Motorola to put both linear and digital functions on one chip. The linear functions contained are high-performance, low-power operational and differential amplifiers.

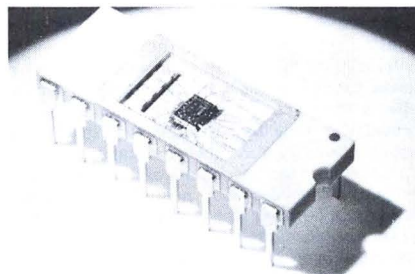
The MC14433 package is a 24-pin dual-inline in either plastic ("P" suffix) or ceramic ("L" suffix). Pricing in quantities of 100 to 999 is \$9.97 for the MC13322P and \$14.95 for the MC14433L. Availability is off-the-shelf from the factory or distributor stock.

For further information contact Technical Communications, Motorola Integrated Circuit Division, 3501 Ed Bluestein Blvd., Austin, TX 78721.

CIRCLE INQUIRY NO. 97

8-Bit D/A Converter Features High Speed, Direct Interface to All Logic Families

A new series of high speed multiplying digital-to-analog converters with direct interface to TTL, ECL, HTL, CMOS and PMOS logic families is now available from Signetics.



Designated NE5007/8 and SE5008, the new converters incorporate advanced circuit design that achieves 85-nanosecond settling time and high swing, adjustable threshold logic inputs to provide full noise immunity.

At -15 volts, for example, logic inputs may swing between -10 volts and $+18$ volts. This makes possible direct interface with CMOS logic, even when the unit is powered from a 5-volt supply.

The 5007/8 units are pin and functionally compatible with monoDAC-08 converters originally introduced by Precision Monolithic Incorporated.

Monotonic multiplying performance in the 5007/8 units is attained over a wide 40 to 1 reference current range. Full-scale current is pre-matched to ± 1 LSB so the need for full-scale trimming is eliminated in most applications. Linearities are as close as 0.19% over the entire operating temperature range, which is -55 degrees C to 125 degrees C for the unit designated SE5008.

Typical applications include converters for servo motors, pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and many other applications where low-cost and high speed D/A conversion is required.

Power supply range is from ± 4.5 volts to ± 18 volts with essentially unchanged performance over the range. The convenient 16-pin plastic DIP package and power consumption of 33 milliwatts with a ± 5 volt supply makes the 5007/8 converters ideal for use in portable equipment and for military/aerospace applications.

The 5007/8 units offer dual complementary outputs that permit differential operation, effectively doubling the peak-to-peak output swing. Output compliance is from -10 volts to $+18$ volts.

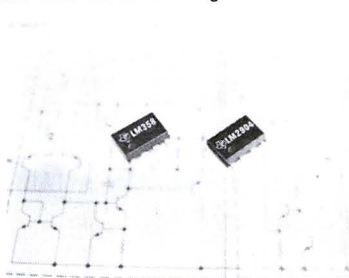
The NE5007/8 and SE5008 converters are available from stock through Signetics and its authorized distributors. Prices in quantities of 100 are \$3.45 for NE5007 and \$3.95 for NE5008.

For further information contact Signetics, 811 East Arques Avenue, Sunnyvale, CA 94086; (408) 739-7700.

CIRCLE INQUIRY NO. 98

Two New Dual OP Amps

Texas Instruments has announced two new dual operational amplifiers, the LM358 and LM2904. Both are second source to the National devices with the same designations.



The two high-gain, frequency-compensated op amps were designed to operate specifically from a single power supply over a wide range of voltages.

The LM358 is available in 8-pin plastic and ceramic DIP and 8-pin metal can packages. It is characterized for 0°C to 70°C. Prices are 67 cents per part in 100 part quantities for the plastic package. (The LM158 and LM258 offer different operating temperature ranges, -55 °C to 125°C and -25 °C to 85°C respectively.)

The LM2904 is also available in 8-pin plastic and ceramic DIP and 8-pin metal can packages. It is characterized for -40 °C to 85°C operation. Prices are \$1.15 each in quantities of 100 for plastic packages.

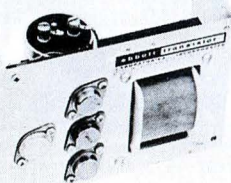
Both devices are available in plastic now at TI distributors. Ceramic and metal can versions will be available soon.

For further information contact Texas Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308, Dallas, Texas 75222 (Attn: LM/358,2904); (214) 238-2955.

EQUIPMENT

Power Module Case Size AAA Triple Output

The "AAA" series of the new NL line provides triple outputs of 5V/3A or either 12V/1.0A \pm 15V/0.8A. Standard input is 115 VAC, 47 to 440 Hz with 220 VAC available at no additional cost. Dual primaries are also available. All units feature tight regulation, low ripple and full load operation at 50°C ambient temperature with de-rating to 40% at 71°C.



Overvoltage protection is standard on 5V outputs and available as an optional feature on the higher voltages. Case size is only 10 1/4 X 4 X 2 1/2 inches with mounting on three surfaces. High quality components are used throughout with conservative design margins to assure high reliability and long life under worst case operating conditions.

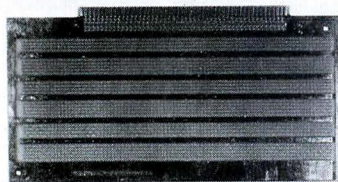
The NL line also includes single, dual and triple output models with power ratings from 15 to 170 watts. Send for Abbott's new 1976-77 Industrial Power Supply Catalog for complete details on this and other lines of power modules. \$69.00 (1-24 pieces) normally from stock.

For further information contact Abbott Industrial Products Division, 639 South Glenwood Place, Burbank, CA 91506; (213) 841-2510, Telex 69-6282.

CIRCLE INQUIRY NO. 99

1010 Prototype Board for ALTAIR and IMSAI

The Tarbell Electronics Model 1010 Prototype Board for the ALTAIR* and IMSAI computers is much better than other available boards.



This board accepts up to 33 14-pin IC's, or a mixture of 40-pin, 24-pin, 18-pin, 16-pin, and 14-pin IC's. It is mainly oriented toward soldering point to point, but wire-wrap may also be used. There are three rows for IC's. The IC's or sockets are inserted from the top, then wires are soldered to the adjacent tabs. The tabs are such that even with 40-pin IC's, there are still two holes left over on each pin for wires. A place for a

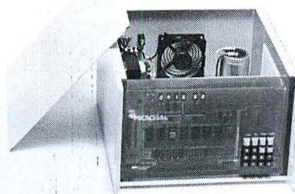
5-volt regulator is also provided. Edge pins are gold-plated. The price is \$28.

*ALTAIR is a trademark/tradename of MITS, Inc. For further information contact Tarbell Electronics, 144 Miraleste Drive #106, Miraleste, CA 90732; (213) 538-4251.

CIRCLE INQUIRY NO. 100

Micro-68b™ Microcomputer

The MICRO-68b comes completely assembled with hexkeyboard, 6 digit LED display, 8K RAM, 1K PROM Monitor system, CRT/TTY/Audio Cassette interface.



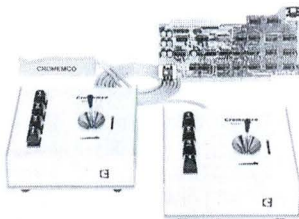
It is housed in a ruggedized aluminum cabinet with a 13 slot exorcisor compatible mother board and 20 amp power supply. The MICRO-68b utilizes the 6800 microprocessor chip set now manufactured by Motorola, AMI, Fairchild, Hitachi and Thompson CSF. The MICRO-68b lists for \$1878.00 and is available from stock.

For further information contact Patti Neumann, Electronic Product Associates, Inc., Director of Marketing, 1157 Vega Street, San Diego, CA 92110; (714) 276-8911.

CIRCLE INQUIRY NO. 101

Joystick Console Gives More Flexibility to Microcomputers

A new 2-axis joystick console has significant features not found in existing joysticks. The new joystick is a console rather than merely a simple 2-input device.



It is called a console because it includes a speaker and speaker amplifier built into the same housing with the joystick. The speaker greatly enhances the usefulness of this over other joysticks because it facilitates such uses as sound effects for computer and other games — and provides an easy way to obtain such features as acoustic warnings in other applications.

Another interesting feature of the new console is that it includes four pushbutton switches. These can be used to add much more flexibility to such applications as using the console for cursor positioning on a color graphics terminal. In such a case the switches can select desired colors.

Cromemco also offers peripherals that simplify application of the joystick. One is a fast 7-channel analog-to-digital I/O card. This unit will directly interface two of the consoles to microcomputers. The I/O is a plug-in card.

Cromemco also offers a color graphics interface known as the TV Dazzler*. This unit allows microcomputers to display memory in color on an ordinary color TV set.

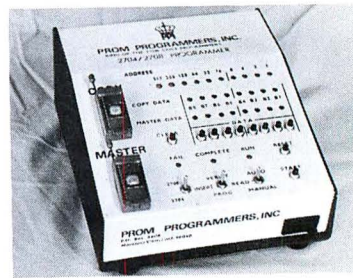
Price of the new console is \$65 in kit form or \$95 in assembled, ready-to-use form. Delivery is 15-30 days.

For further information contact Mr. Joe McCrate, Cromemco, Inc., 2432 Charleston Rd., Mountain View, CA 94043; (415) 964-7400.

CIRCLE INQUIRY NO. 102

Microprocessor System Boards

The line consists of three boards: central processor board, memory board, and interface board all in the standard 100 x 160 mm EUROCARD FORMAT. Each board is pre-assembled with the appropriate mini-wrap I.C. sockets, decoupling capacitors, and 64 pin indirect connector plug. The central processor board, for example, comes complete with two 40 pin, four 28 pin, and four 16 pin sockets; fifty mini-wrap terminal pins, eight mini-wrap test point pins, ten decoupling capacitors, and a 64 pin connector plug.



The CPU board is designed to accommodate the microprocessor chip and the minimum memory, clock and interfacing chips. Space is also available for added discrete components and pots enabling the basic system to operate.

The capacity of the CPU can be extended by adding one or more memory boards, each of which are mounted with eight 28 pin sockets designed to accommodate 8K additional memory per board.

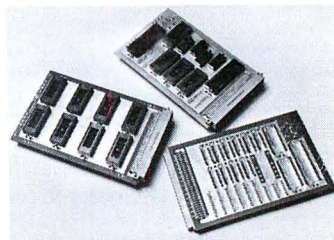
The interface board enables the system to be expanded by providing more comprehensive interfacing and control facilities. In addition to the I.C. sockets, space is also provided for additional discrete components and a crystal permitting the user to construct a crystal controlled clock, which can increase the system's operating speed up to 1 MHz.

For further information contact Vero Electronics Incorporated, 171 Bridge Road, Hauppauge, N.Y. 11787; (516) 234-0400, TWX 510-227-8890.

CIRCLE INQUIRY NO. 103

2708/2704 PROM Emulating Programmer

The lowest priced, highest performance, 2708/2704 PROM programmer is being claimed by PROM PROGRAMMERS, INC.. The King of the Low Cost Programmers. This complete, stand alone, system is priced at \$795 and has the capability of both programming and in circuit emulation.



Programming is accomplished using a master PROM or with the binary switches that have been provided for generating or modifying programs within the internal RAM buffer memory.

Interfacing the Master socket of the unit to the in system socket allows the programmer to emulate a 2708 or 2704 PROM. The RAM in the

programmer makes it easy to alter or edit the program being used. Once the data is correct it can be transferred automatically into a 2708 or 2704 PROM by activating the program cycle in the instrument.

Being about the smallest programmer available anywhere the 2½ X 6 X 8 case will easily fit into a briefcase for use in the field or on a desk for use in the factory. Front panel LED's are provided to indicate the state of the address and data lines for both the Master PROM and the Copy. The Programming algorithm is set to Intel's specifications and takes around two minutes to duplicate a Master.

The system includes a General Purpose Interface that enables the PROM to be programmed from a Microprocessor, Mini Computer, etc.

Also available are stand alone units in the same case as the 2708/2704 for the other UV-erasable PROM's, including the 1702A, 5203, and 5204 PROM's. Erase lamp also available. Delivery is from stock to 30 days.

For further information contact PROM Programmers, Inc., 601 Nandell Lane, Los Altos, CA 94022; (415) 948-0450.

CIRCLE INQUIRY NO. 104

Production-Line 1024 X 1024 Digital Raster Graphics Display System Under \$20,000

GCT-1024 is a 1024 X 1024 digital raster graphics display system. Its ultra-high resolution takes the "stair-step" appearance out of raster displays to minimize distortion and provide greater density detail.



The complete high-performance, 1024 X 1024 digital graphics display system has been available on a production-run basis and is also priced at under \$20,000 (in volume quantities). It includes a unique and proprietary discrete microprocessor that provides instruction times as fast as 150 nanoseconds and 51 mnemonic instructions for increased user programming flexibility.

Coupled with a wide variety of options and accessories such as: a table-mount "joystick" assembly, up to 64-function keyboard units, graphic tablets and cursors, the GCT-1024 is user programmable. Even units with up to 16 gray scales are optionally available.

Applications include functions like Command and Control Process Simulation, Automatic Data Reduction, Computer-Aided Design, Mapping, War Gaming, and Crystallography in such diverse fields as Textiles, Medical, Architecture, Industrial Design, Control Equipment, etc.

Before being officially introduced to the open market the GCT-1024 had already proven its reliability and performance-worthiness in a number of customer installations under stringent-user operating conditions.

For further information contact William Huber, Genisco Computers, 17805-D Sky Park Circle Drive, Irvine, CA 92714; (714) 556-4916.

CIRCLE INQUIRY NO. 105

Low-Cost Sophisticated Mass Storage for Microcomputers from Micro Designs

Recognizing the need for low-cost versatile mass storage for Altair-type 8080 based microcomputers, Micro Designs is offering two new digital cassette mass storage systems with up to

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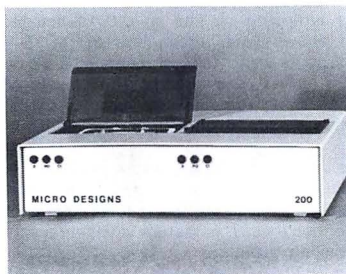
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ASK FOR OUR FREE COMPUTER HOBBYIST BUYERS GUIDE

CIRCLE INQUIRY NO. 39

one megabyte capacity.

An integral part of these ready-to-use systems is their complete file management software which allows the user to manipulate both symbolic and binary files with high-level commands.



The Micro Designs Model 100, a compact unit with a single cassette drive, stores one-half megabyte of data. The disk-like format of the

data on the tape allows access to any single 128 byte record. The data transfer rate is 1000 bytes per second, and the tape may be searched at a rate exceeding 120 inches per second. The dual transport Model 200 puts one megabyte on line.

Both units come fully assembled, and ready for immediate use. The supplied interface board plugs into the main frame motherboard connector to attach the mass storage unit to the computer. To bring up the operating system, the user loads a cassette, and transfers control to the ROM on the interface board; all further tape operations are automatic. Status lights inform the user of relevant tape conditions, and hardware error detection is provided.

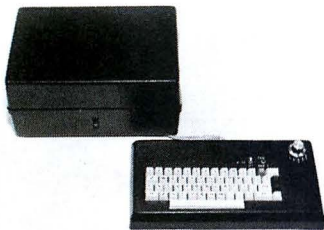
These small table top units sell for \$550 (Model 100) and \$825 (Model 200). Delivery is 30 days.

For further information contact Micro Designs Inc., 1175 Colusa Ave., Berkeley, CA 94707; (415) 526-7794.

CIRCLE INQUIRY NO. 106

Enclosure Kit for the CT-1024 Terminal

PARSEC ELECTRONICS is now marketing an enclosure kit for the SWTPC CT-1024 Terminal System.



A two enclosure design is used to give the terminal suitable protection while retaining the flexibility of a movable keyboard for the user. The two cases are formed from strong, resilient ABS plastic and are color coordinated to blend in with the SWTPC 6800 computer system. The keyboard enclosure has the cutout and mounting pads for the KBD-5 keyboard and a fully enclosed bottom. The main case features mounting pads for the CT-1024 main board, the GT-61 graphics board, the AC-30 cassette interface board and room for their power supplies. The kit includes mounting hardware for all circuit boards, a heatsink for the power supplies and rubber feet for both enclosures.

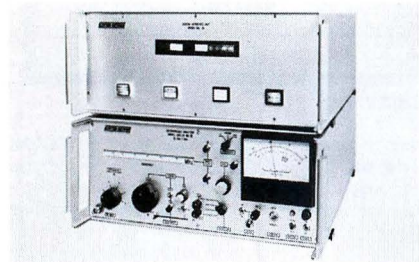
For further information contact PARSEC, P.O. Box A82327, San Diego, CA 92138.

CIRCLE INQUIRY NO. 107

Digital Interface Unit, DIU-25, Interfaces EMC-25 Interference Analyzers, Electronic Calculators and Computers

Model DIU-25 Digital Interface Unit interfaces the popular Electro-Metrics model EMC-25 Interference Analyzer to the Hewlett Packard HP 9825 and other calculators in the HP 9800 series. In addition, it provides a digital interface to all Hewlett Packard mini-computers and the Digital Equipment Corporation's PDP-8 series of mini-computers.

The new Electro-Metrics Interface Unit decodes digital commands from the calculator or computer, issues corresponding instructions to the Electro-Metrics EMC-25 Interference Analyzer, and then converts the resulting EMC-25 data to appropriate digital format. This data is then fed to the calculator or computer for processing. The result is excellent closed-loop control of EMC-25 Interference Analyzer operation in accordance with the stored program.



An optional Operating Software package, the Electro-Metrics OS-25, permits operation of the EMC-25/DIU-25 combination by personnel *without prior programming experience*. Development of additional software by the user is simplified by inclusion within the DIU-25 Digital Interface Unit of numerous hard-wired micro-programs.

Of special note in addition to the EMC-25, the new DIU-25 unit also can control key Electro-Metrics accessory devices. These include programmable attenuators, antenna switching units and X-Y plotters.

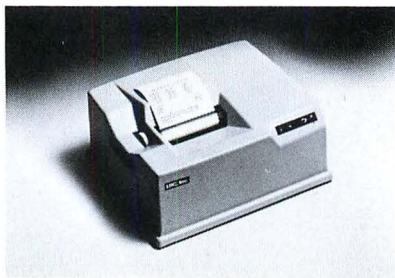
The introductory price is \$14,900 and shipments are available in less than 60 days after the date of order.

For further information contact David Cook, Electro-Metrics Division, 100 Church Street, Amsterdam, N.Y. 12010; (518) 843-2600.

CIRCLE INQUIRY NO. 108

Stand-alone Printer

Model 140 is a 40-column stand-alone printer system with complete electronics which utilizes the same field-proven dot matrix impact printing mechanism which LRC developed and introduced in early 1975.



The system includes a proprietary MOS interface chip which includes a 48-character buffer, a character generator, and complete control logic. Through simple external commands, character width and density may be changed at any time, even during printing. Double-width as well as double-high characters may be generated at any time via simple external instructions.

A long list of available options includes; RS-232-C (or current-loop) communications interface, pin-feed platen, high-speed paper feed, label printing (including label stripping), as well as front-feed document printing.

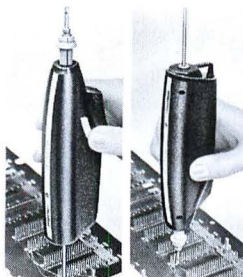
Single-unit price is \$495 with substantial discounts for OEM quantities. Deliveries begin in January, 1977.

For further information contact LRC, Inc., Riverton, Wyoming 82501; (307) 856-6524.

CIRCLE INQUIRY NO. 109

Double-ended Tool Speeds Wire Wrapping; Unwrapping

A new double-ended tool, Model P160-9 from Vector Electronic Company, has a wrapping bit on one end and an unwrapping bit on the other for fast, single-tool wrapped-wire terminations. Designed for use either with Vector's battery-powered P160-4R power tool or for manual wrapping, the tool makes gas-tight terminations on 0.025 inch square posts, using 26 to 30 AWG wire. To remove a wire, the tool is simply turned end for end.



The wrapping bit has an 0.070 inch radius which allows wire termination of 0.025 inch square posts on 0.100 inch centers. A bit depth of 0.56 inches permits three wrap levels. Minimum stripping force for six turns of 26 AWG wire is six pounds; three pounds for 30 AWG wire.

The unwrapping bit has a spring-loaded sleeve that retains and ejects the wire after removal, preventing loose wire from falling among the interconnections. This feature saves time wasted in retrieving the wire.

The P160-9 Wrap-N-Unwrap tool is configured for either left-hand or right-hand manual wrapping and unwrapping. The power tool has a right-hand rotation for wrapping with

the P160-9 tool; however, by inverting the power tool, left-hand unwrapping is achieved.

The P160-9 Wrap-N-Unwrap tool is priced at \$18.40, and the low-cost P160-4R power tool is priced at \$45.68. Both are available from stock.

For further information contact Vector Electronic Company, Inc., 12460 Gladstone Avenue, Sylmar CA 91342; (213) 365-9661, TWX 910-496-1539.

CIRCLE INQUIRY NO. 110

Burn-Out-Proof DC Power Supply

Model 244 MOBIL/COMM Power Supply is a compatible, rack-mountable dc power supply addition to the Hickok CB service system.



The Model 244 MOBIL/COMM Power Supply offers features of particular value to service technicians. The fully-adjustable voltage range of 10.5 to 14.5 volts is accurately metered on large 2 1/2" meter with the calibrated standard 13.8 volt setting clearly indicated. Full adjustability and 0.5% regulation permits duplication of actual storage-battery operating conditions such as low-voltage and over-voltage operation.

Continuous-duty three ampere output is protected against short circuits by fold-back current limiting is that during high current-load conditions that may exist in malfunctioning transceivers the power supply will not shut off, but, automatically reduce the current output to a relatively safe level so troubleshooting can continue with current flowing at a reduced level. When the meter switch is in the AMPS position the output current is indicated with 3% accuracy. The fold-back current limiting is self recovering. After the short circuit is removed the unit returns to normal operation, no fuse to replace, no circuit breakers to reset. All overload conditions are indicated by a front-panel OVERLOAD light.

Output connections to the Model 244 are convenient 5-way binding posts.

The Hickok Model 244 MOBIL/COMM Power Supply is available now at Hickok distributors for \$125.00.

For further information contact Marketing Services Department, Hickok Electrical Instrument Company, 10514 Dupont Avenue, Cleveland, Ohio 44108.

CIRCLE INQUIRY NO. 111

In-Line Digital CB Monitor Provides First Do-It-Yourself Radio Check for 40-Channel CB

The Hickok CB Monitor 38 is a compact, digital-readout CB Monitor which provides display of frequency, power, and SWR.



This is a CB-user version of the precision communication service instruments produced by

Hickok for CB technicians. Designed to be installed in-line between the transceiver and antenna the compact package provides 6-digit frequency readout accurate to 10 parts per million (.001%), 3-digit power output measurement of 1.0 watt to 10.0 watts or if modified 1 watt to 100 watts, accurate to 5%, and 4-digit SWR readings of 1.00:1 to 10.00:1.

The attractively styled package is about the size of a small mobile CB transceiver 6" w x 2 1/4" h x 7" d, and comes complete with all mounting hardware. The CB Monitor 38 can be operated from standard line voltage of 105 to 125 Vac or a 12 volt car battery for mobile application.

In normal operation with either AM or SSB transceivers the CB Monitor 38 will provide continuous digital readout of the frequency output of the transmitter, the power output of the final stages of the transmitter and the functional condition of the antenna system and transmission cable. The CB operator can read the operational condition of his communications system and can take corrective action for maximum effectiveness.

The CB Monitor 38 is available now through Hickok distributors. Suggested retail price is \$279.00.

For further information contact Marketing Services Department, Hickok Electrical Instrument Company, 10514 Dupont Avenue, Cleveland, Ohio 44108.

CIRCLE INQUIRY NO. 112

SOFTWARE

Mupro 8080 Software Programs Now Available for License/Purchase

The BSAL-80 Block Structured Assembly Language programs for use with the 8080 family of microprocessors is now available on a Program License Charge Basis. The programs are fully compatible with muPro-80 and other 8080 Development Systems.

The BSAL-80 Assembler with Relocating/Linking Loader allows 8080 users to write programs in high-level language syntax while retaining the flexibility, program size and execution speed of assembly language. The ability to utilize any of the 8080 machine instructions and to control the use of the architectural features of the 8080 is maintained.

Object code produced by BSAL-80 is in relocatable form, allowing true modular software design and program implementation. The BSAL-80 Relocating/Linking Loader combines individual program modules produced by the BSAL-80 assembler into one executable object module. The linking loader permits the programmer to specify program starting addresses, data starting addresses, module loading sequence and address space for data variables.

The text editor provides a powerful text generation and editing capability. Text manipulation is facilitated by automatic line numbering and a unique command set including ADD, DELETE, LIST, FIND, REPLACE, MODIFY, GATHER, KEEP and SET commands.

The BSAL-80 assembler and loader are provided in 8080 resident or Standard Fortran IV Cross Assembler versions.

Programs are available in paper tape or floppy diskette media. The programs are also provided free of charge with the purchase of the muPro-80, muPro-80E or muPro-80ED Hardware/Software Development Systems.

BSAL-80 Assembler with BSAL-80 Relocating/Linking Loader is \$975. The BSAL-80 Text Editor is \$350. The price for both programs purchased together is \$1,250. The Standard Fortran IV Crossassembler version is \$1,250.00 Delivery is immediate.

JANUARY 1977

Disc/3

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CIRCLE INQUIRY NO. 44

For further information contact Jim Moon, muPro Inc., 424 Oakmead Parkway, Sunnyvale, CA 94086; (408) 737-0500.

CIRCLE INQUIRY NO. 113

AMDASM 2900 Software

A software system to generate microinstructions for use with the Am2900 — AMDASM — system has been developed by Advanced Micro Devices and is now available worldwide through Computer Science Corporation's Infonet Service.

Documentation now available explains how to interact with AMDASM to microprogram all control signals and memory to reduce prototype and develop time for 2900 systems. With the use of variable instruction set microprogramming, field service and enhancements to systems are easy as they require only additional data in the microprogram memory. Automatic documentation for

program changes as well as training, documentation and demonstrations of this assembler reduce lead time and cost of writing microcode.

This microprogram assembler provides software assistance and documentation for writing and modifying microprograms and generating tapes for PROM programmers. AMDASM includes a framework for a common language, automatic accounting information and billing control. Budget limits, character rate option and batch rates make AMDASM cost competitive with in-house versions.

AMDASM is on the time-sharing service of Computer Science Corporation, one of the world's largest software companies. It is accessible from a standard time sharing terminal from most major cities.

For further information contact E. Sopkin, Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, CA 94086; (408) 732-2400.

CIRCLE INQUIRY NO. 114

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Fun and Games Programs Offered with TI SR-52 Calculator Purchase

A library of 20 entertaining and challenging games of skill and chance is being added to the prerecorded programs Texas Instruments Incorporated offers to users of the SR-52 magnetic card programmable calculator.

They will be given (at no cost) to SR-52 purchasers between November 15 and January 15. The calculator sells for \$299.95. After January 15, 1977, the new program library will be available to others at a suggested retail price of \$29.95.

Several games in the library require players to solve puzzles using numbers; others simulate sea battles between two ships, hitting a target with mortar fire, parachute jumping, and landing on Mars. There are also games that allow users to play basketball, football, and baseball.

CODE BREAKER — One game, called Code Breaker, challenges the player to determine which one of the over 3,000 possible four-digit numbers the calculator has generated randomly. The number will not include the same digit twice, nor will zeros be used.

As the player keys in his guess of what the number is, the program and calculator display tells him two things. First, he learns how many of his four digits are in the number he seeks, and are also in the correct position. He also finds out the number of digits which are right but in the wrong position.

For example, a player may be seeking a number like 8954 which the calculator has generated. If his guess is 7685, he discovers that he has two of the digits correct, but both are in the wrong position. If his guess is 8459, he learns he has identified all four digits of the number he seeks, and that two are in the right position and two are not.

While it may seem difficult, players can gain proficiency and learn to break the four-digit code rapidly. If, for example, he is trying to identify 8954, and he keys in 1362, he learns he has not guessed any digits correctly so he can disregard those four digits in his later guesses.

STAR BUSTER — A more difficult game in the library is called Star Buster. It uses ones to represent stars and zeros to signify black holes in a simulated "universe." They are arranged in a three by three matrix and the game begins with one star in the center of the matrix and black holes in each of the other eight surrounding points. The object is to shoot at a single star to create new ones.

The problem is that as a player shoots a star, the space it occupied in the matrix becomes a black hole, but new stars are created in adjacent spaces. Shooting a star in the center of the matrix, for example, creates four new stars in spaces above, below and to the left and right of the center space, which then becomes a black hole. The game ends when a player creates eight stars surrounding one black hole in the center of the matrix.

The game gets complicated because a shot creates two, three, or four stars or black holes depending upon their location within the matrix. A shot at a star, therefore may create new ones in desirable locations, but also may substitute a black hole in a space where the player doesn't want one.

BASKETBALL — The basketball game allows two players to alternate on offense and defense as in a real game, and keeps a running score in the calculator display.

To simulate a play, the player on offense confidentially keys in a number from one to five. After the other player does the same thing, the program determines the play's effectiveness based upon the closeness of the two numbers selected by the players.

For example, "ball" control may switch to the

defense if both players key in the number three. If it is not, probability again determines which of the two players takes over on offense.

Based upon a certain number of plays, the calculator will signal the end of the game by causing the scoring information in the display to flash.

SEA BATTLE GAMES — One of the sea battle games is called Phantom Ship. It simulates a ship within a 100 unit X-Y matrix. After a player fires his first shot, the program tells him how many units — but not the direction — the shot missed.

The player can shoot again, but the program will move the ship five units in any direction before he does. Shots must be within five units to score a minor hit, and five of those disable that ship and replace it with a new one at another location. A direct hit is required to sink the ship.

To obtain the games library, those who purchase an SR-52 between November 15, 1976, and January 15, 1977, return a customer information card enclosed in each SR-52 box to "SR-52 Games Library, P.O. Box 1210, Richardson, TX 75080. The offer is good only in the United States and is void where prohibited by law.

For further information contact Texas Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: SR-52 Games), Dallas, TX 75222; (214) 238-2154.

CIRCLE INQUIRY NO. 115

Calculator Programs for Surveyors

A library of prerecorded surveying programs for use with its SR-52 handheld, card programmable calculator has been introduced by Texas Instruments Incorporated.

The flexible, professional programs give the engineer or surveyor advanced calculating power and fast answers both in the field and office.

Included in the library are programs for traverse, closure, balance, vertical and horizontal curve design, EDM and stadia reductions, intersections, earthwork and borrow pit volumes, triangle and curve solutions.

Along with the prerecorded program cards, purchasers of the library receive a program manual with complete user instructions and printed listings of each program and examples of typical problems.

The library has a suggested retail price of \$44.95. It is the latest addition to TI's series of SR-52 libraries, including those for mathematics, finance, electrical engineering, statistics, aviation, marine navigation, and basic applications.

Users of these programs load data into the calculator memory from a magnetic card smaller than a stick of chewing gum. Then variable data is keyed in for fast solutions to specific problems.

The SR-52 calculator has a suggested retail price of \$299.95.

The programs are designed for use by surveyors, civil engineers, highway design engineers, state and municipal engineers and consultants. They provide these professionals with a calculating capability not available before in this price range.

To enhance its capability for field use a 12 volt chamber adapter (DC9100) is also available as an optional accessory for the SR-52, allowing operation from the cigarette lighter in most automobiles.

For further information contact Texas Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: SR-52 Surveyor Pak), Dallas, TX 75222; (214) 238-2154.

CIRCLE INQUIRY NO. 116

CIRCLE INQUIRY NO. 45

INTEGRATED CIRCUITS

[illegible]

VOLUME SPECIALS

MM5262	2K RAM	1	100
MM5369	Divider	90	50
2102-1	500 NS 1K RAM	2 10	1 40
MM5375AA	Alarm Clock	1 80	1 30
FN0503	50" Display	3 75	2 20
18MHz	Crystal	1 20	89
PD41-1.4	150 NS 4K RAM	2 50	90
MA1002E	5" Alarm Clock Mod.	8 00	7 80
MA1013E	7" Alarm Clock Mod.	11 50	8 95
MM5309	Clock	3 90	2 70
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Other orders please call

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Picture programs.

Section 1 contains 20 business type programs. These programs will be of interest to individuals who have businesses, play the stock market, balance their own checkbooks, do installment buying, figure taxes, etc.

Section 2 is the lighter side of the library as it contains 16 games and 12 picture programs. No computer software library is complete without some fun. Among the games presented in this section is one called Checkers. The game is rather long, but it is virtually machine independent, as it does not use overlay techniques nor use files. Most of the other games included here are as exciting as this version of Checkers. Apparently each program was chosen so as not to mimic others that the reader may have seen or used. The pictures are as unusual in their own way as are the games. Most of the pictures are spread over several pages to show details of the particular picture. The picture programs are very simple and it is an ideal place for the novice to start learning about programming.

Volume Two contains 46 BASIC programs subdivided into two sections (3 & 4) consisting of Math & Engineering programs and Plotting & Statistics programs.

Section 3 contains 23 general usage Math & Engineering programs. Some of these programs will be of use to high school students, professional people, engineers, astronomers, private airplane pilots, etc. Most of these programs are very technical but they can perform everyday calculations quickly and are extremely simple to use.

Section 4 contains 5 direct Plotting programs and 18 Statistical programs. These programs can be readily utilized by a number of people in widely different disciplines from fishermen to statisticians. The data gathered may be from a poll, a census, a test sample or even the number of fish caught on various days. The stat programs will be of invaluable aid to anyone who gathers data of any kind. The plotting routines will be of use to most of the people who use business programs from section 1, Math & Engineering programs from section 3, and Stat programs from this section. The plotting is done on any standard teletype or terminal and does not require a special plotter or plotting terminal.

Appendix A - Volume 2 also includes an Appendix where the BASIC language grammar is defined. All of the BASIC statements used throughout the BASIC programs are defined here. Each statement is explained sufficiently well to enable one unfamiliar with this subset of BASIC to modify any necessary statements so that the program or programs will compile

and/or execute with the BASIC Compiler or Interpreter available with their particular computer. Most of the BASIC Compilers available today that require more than 10K Bytes of storage will execute all of the programs presented in these three volumes with the possible exception of a few of the games and the program "Variable." Multiple line statements are not used in most of the programs and only a few programs are string manipulations extensively. A few of the programs may require more line storage than is available on some of the small Micro-computer systems; these longer programs will not be executable because of the limited amount of memory. However, most of the programs will execute in 10K Bytes of memory or less, thereby making most of the programs in this Library executable in virtually any BASIC speaking computer without any required modifications.

Volume three contains 8 BASIC programs on advanced business programs consisting of Invoice Billing & Accounts Receivable program, Inventory Control program, Payroll with deduction program, Capital Investment-Risk Analysis program, Resource Scheduling program, Transportation cost & scheduling assignment program, Stock Value program and a Bond switch Decision program.



Have you told a friend about INTER-
FACE AGE?

SOFTWARE SECTION

By Robert A. Stevens
Software Editor

FILLING THE SOFTWARE LANGUAGE GAP

INTERFACE AGE takes another step forward in filling the Microcomputer software void. This issue includes 4 articles on software which include 3 major software development program source listings and one BASIC language math function software source listing.

Two BASIC interpreters, one on Tiny BASIC and one on standard BASIC provide conversational language programming capabilities for the SC/MP and 8080 based Microcomputers. National's NIBL TBX Interpreter by Mark Alexander provides conversational language program development for the SC/MP while the LLL's BASIC Interpreter by John Dickinson, Jerry Barber and others provides conversational language program development for the 8080. In addition, both of these highly commented source listings provide a detailed insight into language programming for those of you interested in BASIC language development. The complete NIBL assembly listing is published in this issue while part two of the LLL8080 BASIC Interpreter-BASIC assembly listing without Floating Point is published in this issue. Assembly listings for the other two parts of the LLL BASIC Interpreter will be published in the next two issues of INTERFACE AGE.

A new resident 8080 software package called CONSOL developed by Processor Technology provides a resident software operating system for their new single PCB intelligent Microcomputer Terminal called SOL Terminal Computer. The complete CONSOL assembly listing is published in this issue.

BEST ARTICLE OF THE YEAR AWARD

INTERFACE AGE will bestow an Honorary Award of \$500 value in products advertised in INTERFACE AGE to the author of the best non-commercial Microcomputer article published during the year ending November 1977. The best article of the year award will be picked from the group of the best article of the month awards. Like the best article of the month award, only individuals are eligible for this yearly honorarium. The yearly award is in addition to the monthly award and honorarium given on the page count basis. The yearly award will be judged by the editors of INTERFACE AGE and will be announced in February 1978 issue of INTERFACE AGE.

BEST ARTICLE OF THE MONTH AWARD UP-DATE

Starting in last month's issue, INTERFACE AGE will bestow an Honorary Award of \$100.00 to the author of the best non-commercial Microcomputer article of the month. Only individuals are eligible for this monthly honorarium. This monthly award is in addition to the honorarium given on the page count basis. Microcomputer articles may be on hardware, software or a combination hardware-software and will be judged by the INTERFACE AGE readership.

All valid bingo vote cards must be postmarked prior to 12:00 P.M. of the last day of the month *following* the issue date of the related magazine.

DON'T FORGET TO VOTE

Help INTERFACE AGE determine the type of articles you want to see published in the future by casting your vote of 10 points for the article or articles (by vote splitting) you liked best. Feedback will provide encouragement to authors and will help make the INTERFACE AGE the Microcomputer magazine of the industry. See the December 1976 issue for bingo card voting details.

INTERFACE AGE WILL PAY UP TO \$50/PAGE FOR SOFTWARE

INTERFACE AGE is continually soliciting original unpublished quality documented highly commented source/object code software listings and software technical articles for publishing in the INTERFACE AGE. Manuscript text must be typed double spaced with wide margins. Figures, tables, flow diagrams and charts must be numbered and submitted on separate sheets of white bond paper (Send original copy only). Program listings must be printed on white clean paper using a new black ink ribbon, and please, if possible, supply a punched paper tape assembly (source-object) code listing + source code listing + object code dump with your hard copy. Be sure to record your name, company and office and home telephone numbers on all material submitted to the software editor. Also include statement in cover letter allowing INTERFACE AGE and the Microcomputer Software Depository to publish and distribute copies of your software program. Include a prepaid postage stamped envelope with your return address only if you want your manuscript returned, in the event that the submitted article is not accepted for publication.

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CIRCLE INQUIRY NO. 43

upon technical content, manuscript preparation and subject suitability for publication in INTERFACE AGE. Honorariums range from \$15.00 to \$50.00 per typeset magazine page. In addition, starting with this issue, the best article of the month submitted will receive a \$100 bonus. INTERFACE AGE's readership will determine by vote which is the best article. (See best article of the month award). All software submitted to INTERFACE AGE will be deposited in the Microcomputer Software Depository (MDS) for low cost distribution.

Address all software correspondence to
 R.A. Stevens
 Software Editor c/o INTERFACE AGE Magazine
 2361 E. Foothill Blvd.
 Pasadena, CA 91107 or call (213) 449-1655.

INTERFACE AGE SOFTWARE SHOPPING LIST

Now that INTERFACE AGE has expanded the Microcomputer software coverage and developed a large appetite for good software, your programs and application software is badly needed to quench this enlarged software appetite. This software shopping list includes the following:

- Microcomputer Development Software
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- Hardware Control Programs
- Personal Bookkeeping Programs
- Personal Investment Programs

- Stock Market programs
- Small Fry Educational Programs
- Software Communications Protocol Programs
- Off-Line Software Mass Storage Format Control Programs
- Game Programs
- Math Plotting Programs
- Statistics Programs
- Engineering Programs
- You Name It Programs

SECOND CALL FOR INFORMATION ON BASIC PROGRAMMING LANGUAGES

INTERFACE AGE is conducting a survey on the characteristics and programming power of Microcomputer BASIC conversational programming languages. This survey includes Tiny BASIC (TB), Tiny BASIC Extended (TBX), Standard BASIC (SB), Standard BASIC Extended (SBX) and Business BASIC (BB) languages. One of the main objectives of this survey is to highlight the correlation between BASIC languages in order to provide insight for running a BASIC application program on any of the different BASIC languages. If you have developed, helped develop or modified any BASIC type of programming language for any Microcomputer please contact or send hard copy of grammar, users manual and any supporting documentation to:

Robert A. Stevens
 Software Editor
 INTERFACE AGE
 2361 E. Foothill Blvd.
 Pasadena, Calif., 91107
 Or Call (213) 449-1655

Please include your home and work telephone numbers (for coordination) with all correspondence.

INEXPENSIVE MICROCOMPUTER SOFTWARE

The Microcomputer Software Depository (MSD) will act as repository for source and object code tapes. Programmers wishing to contribute programs to the public domain but who do not want to bother with distribution, may do so by forwarding appropriate documentation including short descriptive write-up and punch paper tape copy of program if possible or cassette copy to MSD. There is no membership fee for access to the public domain paper tapes (PDT) from MSD.

Anyone may obtain copies of these PDT software packages by prepaying a small fee with the order to cover duplication, postage and handling cost. Prices will be listed periodically in INTERFACE AGE. Typical cost for a short program will be approximately \$2.00 (\$2.00/ounce) + tax, postage and handling. As a convenience MSD will also provide punched paper tape copies of vendor supplied software packages (VSP) that will be sold at vendor suggested sale prices. For a current copy of the available software from the Microcomputer Software Depository (MDS) send a check for \$1.00 with a prestamped return envelope to MSD.

Support MSD to build a software library by sending

copies of your documented software programs including short description, flow diagrams and punched paper tape source code and object listings if possible or cassette tape copy for low cost distribution to the following address

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MICROCOMPUTER SOFTWARE DEPOSITORY PROGRAM LISTING

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PROGRAM MEDIA	NOTES
PTAC PAPER TAPE ASSEMBLY CODE	* CALIF. SALES TAX REQUIRED FROM RESIDENCE OF CALIF.
PTSC PAPER TAPE SOURCE CODE	: USA POSTAGE + HANDLING OR THIRD CLASS USA POSTAGE + HANDLING OR SURFACE RATE FOREIGN POSTAGE @
PTOC PAPER TAPE OBJECT CODE	THREE TIMES THIRD CLASS USA POSTAGE RATE (STANDARD) OR SURFACE RATE FOREIGN POSTAGE @ FIVE TIMES USA POSTAGE RATE (ALTERNATE)
PTBC PAPER TAPE BASIC CODE	< NEW PROGRAM LISTING
PTAL PAPER TAPE ASSEMBLY LISTING	% VENDOR SOFTWARE PACKAGE - ALL OTHER PROGRAMS ARE PUBLIC DOMAIN SOFTWARE WITH THE ONLY RESTRICTION THAT THESE PROGRAMS ARE NOT TO BE SOLD IN ANY FORM AT ANY PRICE.
PTSL PAPER TAPE SOURCE LISTING	
PTOL PAPER TAPE OBJECT LISTING	
PTOD PAPER TAPE OBJECT DUMP	
PTBL PAPER TAPE BASIC LISTING	
CTAL CASSETTE TAPE ASSEMBLY LISTING	
CTSL CASSETTE TAPE SOURCE LISTING	
CTOL CASSETTE TAPE OBJECT LISTING	
CTOD CASSETTE TAPE OBJECT DUMP	
CTBC CASSETTE TAPE BASIC CODE	
CTAL CASSETTE TAPE BASIC LISTING	
HCAC XEROX HARD COPY OF ASSEMBLY CODE	
HCSC XEROX HARD COPY OF SOURCE CODE	
HCOC XEROX HARD COPY OF OBJECT CODE	
HCBC XEROX HARD COPY OF BASIC CODE	
HCAL XEROX HARD COPY OF ASSEMBLY LISTING	
HCSL XEROX HARD COPY OF SOURCE LISTING	
HCOL XEROX HARD COPY OF OBJECT LISTING	
HCOD XEROX HARD COPY OF OBJECT DUMP	
HCOL XEROX HARD COPY OF BASIC LISTING	
TXTX XEROX HARD COPY OF PRINTED TEXT	
PTTL PAPER TAPE TEXT LISTING	
CTTL CASSETTE TAPE TEXT LISTING	
MAN MANUAL	

SUFFIX C = HAND ASSEMBLED CODE
SUFFIX L = COMPUTER FORMATTED LISTING
SUFFIX D = CODE DUMP IN OCTAL OR HEX

DEFINITIONS:

ASSEMBLY LISTING: COMPUTER ASSEMBLED SOFTWARE PROGRAM LISTING THAT INCLUDES SYMBOLIC ASSEMBLY LANGUAGE SOURCE CODED INSTRUCTIONS WITH COMMENTS PLUS EQUIVALENT MACHINE LANGUAGE OBJECT CODED INSTRUCTIONS AND MEMORY ADDRESS ASSIGNMENTS FOR EACH INSTRUCTION (SOURCE + OBJECT).

ASSEMBLY CODE: SAME CONTENT AS ASSEMBLY LISTING BUT HAND ASSEMBLED.

SOURCE LISTING: SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT INCLUDES ASSEMBLY LANGUAGE SOURCE CODED INSTRUCTIONS WITH COMMENTS. SOMETIMES, LINE STATEMENT NUMBERS ARE INCLUDED FOR EACH INSTRUCTION.

SOURCE CODE: SAME CONTENT AS SOURCE LISTING BUT HAND ASSEMBLED.

OBJECT LISTING: SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT ONLY INCLUDES MACHINE READABLE OBJECT CODED INSTRUCTIONS AND MEMORY ADDRESS ASSIGNMENTS.

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CODE: HAND ASSEMBLED CODE (SOURCE, OBJECT, OR ASSEMBLY CODE).

LISTING: COMPUTER FORMATTED LISTING.

DUMP: COMPUTER MEMORY DUMP.

MSD PROGRAMS

CPU TYPE	SYMBOLIC NAME	DESCRIPTIVE NAME	MSD # & MEDIA	R F V	PRICE IN \$	+ CALIF. TAX(*)	+ USA POSTAGE(*)
6502	APPLECD	6502 APPLF COMPUTER DISASSEMBLER BY ALLEN BAUM & STEPHEN WOZNIAK-INTERFACE AGE, SEPT. 1976, VOL.1, #10.	1-TEXT 1-HCAL		1.00+0.06+0.50	INC. WITH TEXT	
8080	LPTIHF	LOAD 8080 PAPER TAPE IN INTEL HEX FORMAT BY BURT HASHIZUME-INTERFACE AGE, OCT. 1976, VOL.1, #11.	2-PTAL 2-TEXT 2-HCAL	0	2.00+0.12+1.00	INC. WITH TEXT	
8080	BFWDA	8080 BINARY FILFS WITH OPTIONAL AUTOSTART BY WILLIAM H. JORDAN-INTERFACE AGE, OCT. 1976, VOL.1, #11.	3-PTAL 3-PTOD 3-TEXT 3-HCAL	0	2.00+0.12+1.00	INC. WITH TEXT	
6800	MINOPS	MIN OPERATING SYSTEM BY ED KEITH & DENNIS HESCOX-INTERFACE AGE, OCT. 1976, VOL.1, #11. PTAL+ INCLUDES OPERATING INSTRUCTIONS, PAPER TAPE FORMAT AND SAMPLE RUN	4-PTAL+ 4-PTOD 4-TEXT 4-HCAL	0	2.00+0.12+1.00	INC. WITH TEXT	
8080	DRBDP	DR. BEATTIE'S BASIC DIET PLANNING BY DR. BEATTIE-INTERFACE AGE, OCT. 1976, VOL.1, #11.	5-TEXT 5-HCSL 5-PTSL	0	1.00+0.06+0.50	INC. WITH TEXT	3.00+0.18+1.00
6800	EZMERPS	ECHO 1, ZERO MEMORY, ECHO REVERSE & PRINT SUBROUTINES BY HOWARD BERENSON-INTERFACE AGE, OCT. 1976, VOL.1, #11.	6-PTAL 6-TEXT 6-HCAL	0	2.00+0.12+1.00	INC. WITH TEXT	
8080	ESP-1	ESP-1 SOFTWARE PACKAGE BY MICHAEL SHRYAKER-INTERFACE AGE, OCT. 1976, VOL.1, #11. PTGR IS PAPER TAPE COPY OF GRAMMAR.	7-PTOD 7-MAN 7-CTOD 7-MAN 7-PTGR 7-TFXT	% 0 0 0 0 0	30.00+1.00+1.50	INC. WITH PTOL	30.00+1.00+1.50 INC. WITH CTOD 5.00+0.30+1.50 INC. WITH PTGR
8080	PTSP-1	PROCESSOR TECHNOLOGY SOFTWARE PACKAGE NO. 1 SUMMARY BY R. A. STEVENS-INTERFACE AGE, OCT. 1976, VOL.1, #11.	8-PTTL 8-TEXT	% 0	1.00+0.06+0.60	INC. WITH PTTL	

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8080	FRAMMT	EXHAUSTIVE 8080 RAM MEMORY TEST PROGRAM BY T.F. THAVIS - INTERFACE AGE, NOV. 1976, VOL.1, #12.	9-PTAL	0	2.00+0.12+0.50	8080	LLBL	LLL 8080 BASIC INTERPRETER GRAMMAR BY JERRY BARBER & ROYCE FCKARD - SUBMITTED BY F.R. FISHER - INTERFACE AGE, DEC. 1976, VOL.1, #13 (PART 1). PART 2 PUBLISHED JAN. 1977, VOL.2, #1. TEXT1 IS PART 1, TEXT2 IS PART 2 AND HCAL2 IS FULL SIZE XEROX COPY OF BASIC ASSEMBLY LISTING WITHOUT FLOATING POINT.	28-TEXT1 < 0	2.00+0.12+1.25
			9-PTOD		INC. WITH PTAL				28-HCAL2 <	5.00+0.30+2.00
			9-TEXT		1.00+0.06+0.50				28-TEXT2	INC. WITH HCAL
			9-HCAL		INC. WITH TEXT					
			9-HC0D		INC. WITH TEXT					
6800	MEMDMP-1	SWTPC 6800 MEMORY DUMP PROGRAM MEMDMP-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	10-PTAL	0	2.00+0.12+1.00					
			10-PTSL <	0	2.00+0.12+1.00					
			10-PTOD <		INC. WITH PTSL					
			10-TEXT		1.00+0.06+0.75					
			10-HCAL		INC. WITH TEXT					
6800	ROBIT-1	SWTPC 6800 ROTATING BIT RAM MEMORY DIAGNOSTIC PROGRAM ROBIT-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	11-PTAL	0	2.00+0.12+1.00	SC/MP NIBL	NIBL-NATIONAL'S TINY BASIC GRAMMAR FOR SC/MP BY PHIL ROYBAL - INTERFACE AGE, DEC. 1976, VOL.1, #13. ASSEMBLY LISTING PUBLISHED JAN. 1977, VOL.2, #1.	29-TEXT < 0	2.00+0.12+1.25	
			11-PTSL <	0	2.00+0.12+1.00			29-HCAL <	10.00+3.00+2.00	
			11-PTOD <		INC. WITH PTSL			29-PTSL <	10.00+3.00+2.00	
			11-TEXT		1.00+0.06+0.75			29-PTOD <	5.00+1.50+1.00	
			11-HCAL		INC. WITH TEXT					
6800	MEMCON-1	SWTPC 6800 SHORT MEMORY ADDRESS CONVERGENCE PROGRAM MEMCON-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	12-PTAL	0	2.00+0.12+1.00	SC/MP MWBAGELS	BAGELS BY DR. MARVIN WINZINREAD BY PERMISSION & COURTESY OF NATIONAL SEMICONDUCTOR - INTERFACE AGE, DEC. 1976, VOL.1, #13.	30-PTBL < 0	2.00+0.12+1.00	
			12-PTSL <	0	2.00+0.12+1.00					
			12-PTOD <		INC. WITH PTSL					
			12-TEXT		1.00+0.06+0.75					
			12-HCAL		INC. WITH TEXT					
6800	RJIR	BLACKJACK IN BASIC PROGRAM RY ED KEITH & DENNIS HESCOX. THE RJIR PAPER TAPE OBJECT CODE REQUIRES ROBERT UITERWYK'S SWTPC MICROBASIC OPERATING SYSTEM-INTERFACE AGE, NOV. 1976, VOL.1, #12. PTBL+ INCLUDES SAMPLE RUN, INSTRUCTIONS, LIST OF VARIABLES AND LIST OF ROUTINES.	13-PTSL <	0	5.00+0.30+1.00	8080	AMS80	AMSAT 8080 STANDARD DEBUG MONITOR BY RICHARD C ALLEN & JOE KASSER - BYTE # 13, SEPT. 1976, VOL.2, #1. SUBMITTED BY JOE KASSER.	31-PTSL < 2	10.00+0.60+2.00
			13-PTBL <		6.00+0.36+1.00			31-PTOD <	3.00+0.18+1.75	
			13-PTOD		6.00+0.36+0.75					
			13-TFXT		1.00+0.06+0.50	6800	BAFCMP	BASIC ALGORITHMS FOR COMMON MATH FUNCTIONS BY MICHAEL P. BURTON - INTERFACE AGE, JAN. 1977, VOL.2, #1.	32-PTBL < 1	3.00+0.24+1.00
			13-HCBL		INC. WITH TEXT			32-TEXT <	1.00+0.06+0.25	
			13-HC0D		INC. WITH TEXT					
6502	RFPK	REVISED FLOATING POINT ROUTINES FOR 6502* BY ROY KANKIN & STEVE WOZNIAR - INTERFACE AGE, NOV. 1976, VOL.1, #12. NOTE * - ORIGINAL MATH PACKAGE FIRST APPEARED IN DR. DORR'S JOURNAL, AUG. 1976, VOL.1, #7.	14-PTOD	1	3.00+0.18+0.60					
			14-PTAL		9.00+0.54+1.50					
			14-PTSL <		9.00+0.54+1.50					
			14-TEXT		1.00+0.06+0.50					
			14-HCAL		INC. WITH TEXT					
6800	HISPDMP	HIGH SPEED DOUBLE PRECISION MULTIPLICATION SUBROUTINE HISPDMP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	15-PTAL	0	2.00+0.12+0.50					
			15-TEXT		1.00+0.06+0.50					
			15-HCAL		INC. WITH TEXT					
6800	DIV16	REENTRANT 16 BIT DIVIDE SUBROUTINE - DIV16 BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	16-PTAL	1	2.00+0.12+0.50					
			16-TEXT		1.00+0.06+0.50					
			16-HCAL		INC. WITH TEXT					
6800	KENTMUP	REENTRANT DOUBLE PRECISION MULTIPLICATION SUBROUTINE KENTMUP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	17-PTAL	0	2.00+0.12+0.50					
			17-TEXT		1.00+0.06+0.50					
			17-HCAL		INC. WITH TEXT					
8080	HOMEK	COMPUTER OR CONTROLLER BY TERRY BENSON, INTEL - INTERFACE AGE, SEPT. 1976, VOL.1, #10.	18-PTAL	0	2.00+0.12+0.50					
			18-PTSL		2.00+0.12+0.50					
			18-TEXT		1.00+0.06+0.50					
			18-HCAL		INC. WITH TEXT					
8080	LCST	STARTRK BY LYNN COCHRAN-INTERFACE AGE, JUNE 1976, VOL.1, #7.	19-PTSL	0	2.00+0.12+0.75					
			19-TEXT		1.00+0.06+0.50					
			19-HCBL		INC. WITH TEXT					
8080	WSPG	WORD SEARCH PUZZLE GENERATOR BY RICHARD S. EDELMAN - INTERFACE AGE, JULY 1976, VOL.1, #8.	20-PTBL	0	2.00+0.12+0.75					
			20-TFXT		1.00+0.06+0.50					
			20-HCBL		INC. WITH TEXT					
8080	PGRIOKHY	BIOIRHYTHM BY PAUL GREEN - INTERFACE AGE, AUG. 1976, VOL.1, #9.	21-PTSL	0	2.00+0.12+0.75					
			21-TEXT		1.00+0.06+0.50					
			21-HCBL		INC. WITH TEXT					
8080	WDBIOKHY	BIOIRHYTHMS IN PRACTICE BY WILLIAM L. DONHAN, M.D. - INTERFACE AGE, AUG. 1976, VOL.1, #9.	22-PTBL	0	2.00+0.12+0.75					
			22-TEXT		1.00+0.06+0.50					
			22-HCBL		INC. WITH TEXT					
8080	RFPJ	BLACKJACK BY RICHARD S. EDELMAN - INTERFACE AGE, AUG. 1976, VOL.1, #9.	23-PTBL	0	2.00+0.12+0.75					
			23-TEXT		1.00+0.06+0.50					
			23-HCBL		INC. WITH TEXT					
8080	BLUFF	BLUFF BY PHIL FELDMAN & TOM RUGE - INTERFACE AGE, SEPT. 1976, VOL.1, #10.	24-PTBL	0	2.00+0.12+0.75					
			24-TEXT		1.00+0.06+0.50					
			24-HCBL		INC. WITH TEXT					
6800	KARSIMB	RELATIVE ADDRESS BACK-STEPPER IN MICRO-BASIC BY J. HUFFMAN - INTERFACE AGE, DEC. 1976, VOL.1, #13.	25-PTSL <	0	2.00+0.12+0.75					
			25-HCBL <		1.00+0.06+0.25					
			25-TEXT <		INC. WITH HCBL					
6800	TEFT6800	TEXT EDITOR FOR THE SWTPC-6800 BY MARK ROSEKROHN - INTERFACE AGE, DEC. 1976, VOL.1, #13.	26-PTAL <	0	10.00+0.36+2.00					
			26-PTOD <		5.00+0.30+1.25					
			26-HCAL <		2.00+0.12+1.25					
8080	WPATHX	WANG'S PALO ALTO TINY BASIC BY ROGER KAUSKOLR - INTERFACE AGE, DEC. 1976, VOL.1, #13.	27-PTSL <	0	10.00+0.60+2.00					
			27-PTOD <		5.00+0.30+1.50					
			27-HCAL <		2.00+0.12+1.50					
			27-TFXT <		INC. WITH HCAL					
			27-HCBL <		2.00+0.12+1.00					

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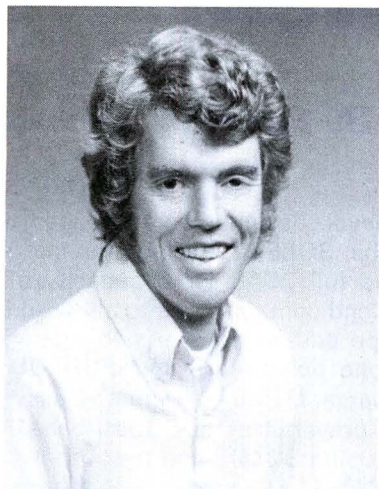
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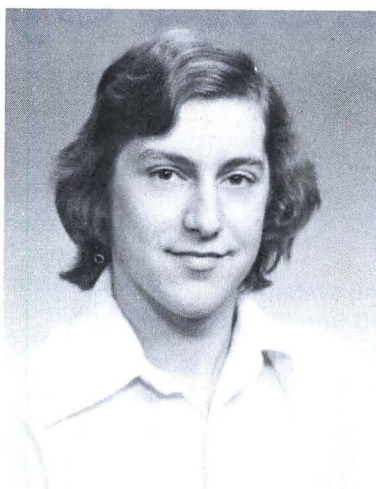
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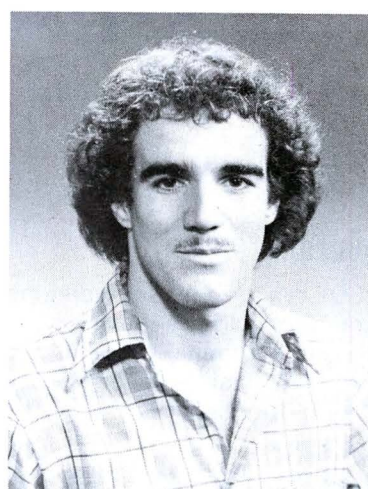
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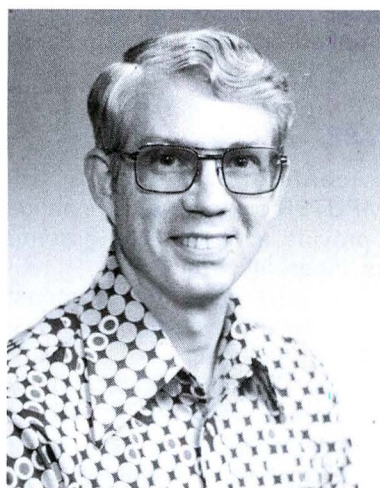
Mike Eusey



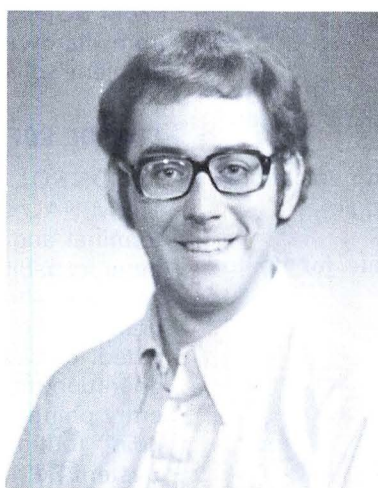
Steve Zook



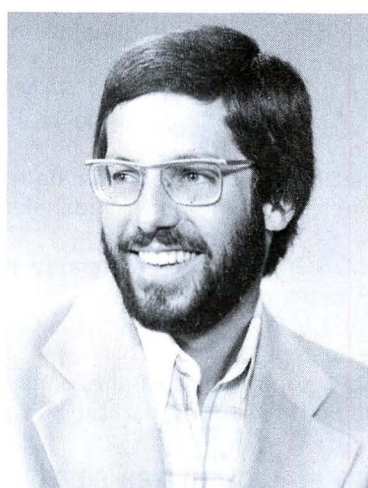
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Consol 1K Resident Operating System

By Processor Technology
Emeryville, CA

INTRODUCTION

CONSOL is a resident software operating system for Processor Technology's new single PCB intelligent microcomputer terminal product called SoL Terminal Computer™. The basic SoL Terminal Computer includes the following functional sections;

- 8080A CPU
- 1K bytes of static, low power RAM
- UART controlled RS-232 and 20 ma TTY serial I/O port with multiple baud rates of 75 → 9600 - Switch selectable.
- Video display circuit identical to the VDM-1 sold by Processor Technology. The video display section includes its own 1K bytes of RAM refresh memory. This RAM is in addition to the 1K RW RAM program memory.
- Parallel input-output port for data communications with fully implemented handshaking logic.
- ASCII Keyboard input port.
- PROM/ROM plug-in personality module for up to 2048 bytes of stored program.
- 300 or 1200 baud rate Kansas City Standard Audio cassette tape interface.
- MIB bus compatibility and expansion capability with all Altair/IMSAI/PTC bus plug-in products.

SOL TERMINAL COMPUTER SOFTWARE CONFIGURATIONS

The SoL Terminal Computer™ can be configured by plug-in resident software modules as a stand alone microcomputer or as an intelligent remote editing terminal.

Basic system operating modes are stored in ROM or PROM on plug-in personality modules with a capacity of up to 2048 words. These modules may be changed in a few seconds to totally reconfigure the system for different applications. Other operating programs, such as BASIC AND FOCAL High level languages, can be loaded automatically into read/write memory (RAM) from cassette tape or floppy disc.

Software control programs for the operation of SoL are designed for three different levels of use. The first level program, CONSOL™, is contained in 1K of PROM and is designed to allow simple terminal operations. In addition, CONSOL allows direct control of the basic computer functions for entering data to, or examining data in, any memory location, or executing a program stored at a known location in memory.

The second level, designed for advanced terminal operations, is the SOLED™ editing terminal system. SOLED uses the full 2048 word capacity of a personality module and contains code to allow screen, file and cassette tape editing/transmission operations.

The stand-alone operating system, SOLOS™, turns the SoL into a versatile computer that is easy to use, but every bit as powerful as any 8080-based system available today. Using SOLOS and the built-in cassette interface, BASIC can be loaded in less than a minute following power-on. BASIC programs can be both saved and executed from cassette. The SoL operating under SOLOS, brings true 8080 computer power away from hardware tinkering to direct application and problem solving.

CONSOL SOFTWARE

CONSOL is configured to allow the SoL TERMINAL/COMPUTER to operate as a standard CRT terminal and to provide access to the essential computer capabilities inherent within SoL. The CONSOL software allows self test and small diagnostic programs to be entered to the system memory and executed thus providing verification of correct system operation. In addition, CONSOL contains standardized entry points for all normal I/O operations. These entry point routines are common with each of the SoL System Software allowing each personality module in the SoL product line to interface with external programs in an almost identical manner.

A cassette read routine is included in the CONSOL module software allowing SoL System Software to be loaded and run in a SoL System with additional memory. SoL System Software includes BASIC, FOCAL, a Scientific Calculator and numerous "game" packages including an 8K assembly language version of STARTREK called TREK80.

CONSOL OPERATION

When power is applied to the SoL unit, CONSOL initializes the system ram area, clears the screen, and enters the terminal mode.

In this mode the SoL System acts as a standard CRT terminal sending keyboard data to an output port and displaying received data on the screen. The COMMAND KEYS of the keyboard are not transmitted to the output port but are interpreted as direct internal operation keys. CURSOR MOVEMENT, HOME and CLEAR SCREEN all operate in this manner, while

SOFTWARE SECTION

MODE causes an immediate change in the operation of the SoL Terminal Computer.

When the MODE key is depressed CONSOL issues a prompt (>) and waits for a command line to be entered via the keyboard. The SoL is now operating as a computer and is ready to accept one of the following commands:

D ump	Dump memory locations to screen
E nter	Enter data to memory
E Xecute	Execute a program in external memory
B asic	Execute a program located at address zero
T erminal	Return to terminal mode
T load	Load program or data from cassette tape
M ODE	Press key to start new command line

CONSOL COMMANDS

The seven SoL CONSOL commands are defined in the following:

DUMP <addr> <addr>

The DUMP command displays memory data on the screen in ASCII Hexidecimal representation. As with all SoL commands the command is recognized by the first two characters and up to ten additional characters can be input without an error being forced. Thus, DU; DUST; DUMP; DUMPTHESE would all be recognized as being a DUMP command.

At least one address must follow the command or an error will result. Entering the command DU followed by addr will result in the data at 'addr' being displayed

MICROCOMPUTER DEVELOPMENT SOFTWARE

on the screen. If two addresses are defined then all values from the first address to the last address will be displayed. The following example shows the DUMP command with the start and terminating addresses specified;

DUMP 0 EF

Up to ten blanks may be inserted between each parameter without forcing an error condition. Errors are flagged by a question mark (?) replacing the character where the error occurred. For example if the DU command were given without an address, the question mark would appear ten spaces to the right of the 'U' character of the dump command.

ENTER addr

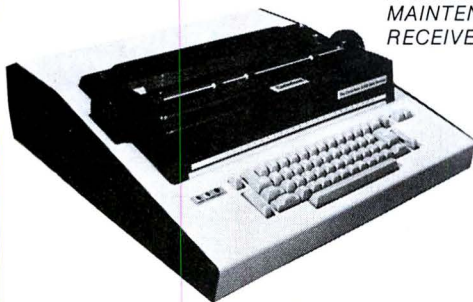
The enter command places sequential bytes into memory beginning at the specified address. Data, represented as hexadecimal values, are entered from the keyboard for storage in memory. Values are entered one line at a time with each line terminated by a carriage return or linefeed. The ENTER command function itself is terminated with a slash (/) and the CONSOL operating system returns to the command mode when the slash is encountered.

Data input lines are terminated with a carriage return or line feed. If the terminator is a C/R, CONSOL will erase all characters from the current cursor location to the end of the screen line. In this case, all valid input should be to the left of the cursor. If an error occurred during input the cursor may be moved back to

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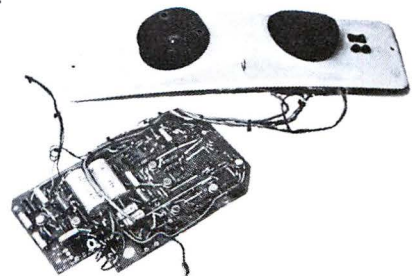
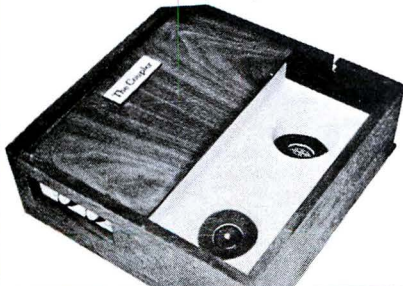
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the left to correct the error.

TLoad <speed>

CONSOL includes routines to read standardized Software from cassette tape. This standardized software is recorded on tape with a sixteen byte header that includes NAME, LOAD INFORMATION, FILE TYPE and execute address. CONSOL, because of space limitations, is unable to search for a program or file by name. After receiving the TLOAD command, CONSOL locates the next available data, uses the header information and loads the file to memory.

After loading the data, CONSOL returns to the command mode where the EXEC command can be used to execute the just loaded program. In addition, a return can normally be made to the command mode by pressing the MODE key. Program Space limitations again limited the mechanization of the escape function during the header search, so if the operation software system locks up in this routine the standard SoL restart must be used to escape.

The Audio Cassette Interface electronics within the SoL will record or receive data at either of two standard speeds. TLOAD will accept a parameter to select this speed, 0 being high speed and 1 being low (300 and 1200 bits per second). If no parameter is given, CONSOL will default to high speed operation as all standard SoL-System Software is recorded at this speed.

EXecute addr

The execute command is used to run programs located in external memory. CONSOL branches to the external routine in a manner similar to a CALL so that the program can return to the command mode using a standard RET instruction if normal stack operations are used.

Basic

The BASIC command is provided for executing programs whose starting address is 0. (Such as SoL-BASIC5).

STANDARD I/O ROUTINES

All SoL System personality modules contain similar I/O code for input/output operations. CONSOL, using 1K of memory, has routines for KEYBOARD and SERIAL PORT input as well as SERIAL and VIDEO DISPLAY OUTPUT. Although the same code for SOLOS and SOLED contains expanded functions, the I/O operations appear almost identical when used with external software.

SoL BASIC5 for example performs all I/O using the jump table of the personality modules. Thus, without altering BASIC the user may output to either the serial port or to the display screen. Provision is also made within BASIC to programatically change to any of the four available Input or Output options. CONSOL is of course limited to the two provided.

*** ALS-8 PROGRAM DEVELOPMENT SYSTEM ***

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PROCESSOR TECHNOLOGY CORP.
6280 HOLLY STREET
EMERYVILLE, CALIF. 94608

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C640	#160 *	VIDEO DISPLAY DRIVER ROUTINES	C11C C8	#J35	RZ	HUM RIGHT LAN RE DEF
C640	#161 *		C11D JC	#J36	INR	A
C640	#162 *		C11E C3 13 C1	#J37	JMP	PCUR
C640	#163 *	THESE ROUTINES ALLOW FOR STANDARD VIDEO TERMINAL	C121	#J38 *		
C640	#164 *	OPERATIONS. ON ENTRY, THE CHARACTER FOR OUTPUT IS IN	C121	#J39 *	ROUTINE TO CALCULATE SCREEN ADDRESS	
C640	#165 *	REGISTER B AND ALL REGISTERS ARE UNALTERED ON RETURN.	C121	#J40 *		
C640	#166 *		C121	#J41 *	ENTRY AT: RETURNS:	
C640	#167 *	THE "CONSUL" VERSION OF THIS ROUTINE IS A MINIMUM	C121	#J42 *		
C640	#168 *	IMPLEMENTATION OF ROUTINES ORIGINATED BY:	C121	#J43 *	VDADD CURRENT SCREEN ADDRESS	
C640	#169 *		C121	#J44 *	VDADD ADDRESS OF CURRENT LINE, CHAR 'C'	
C640	#170 *		C121	#J45 *	VDAD LINE 'A', CHARACTER POSITION 'C'	
C640	#171 *	IAN KETTLEBOROUGH	C121	#J46 *		
C640	#172 *	OF	C121 3A 00 C8	#J47 VDADD	LDA NCHAR	GET CHARACTER POSITION
C640	#173 *	COLLEGE STATION, TEXAS	C124 4F	#J48	MOV C,A	'C' KEEPS IT
C640	#174 *	SOLDS AND SOLED CONTAIN THE ESC SEQUENCES AND OTHER	C125 3A 01 C8	#J49 VDADD	LDA LINE	LINE POSITION
C640	#175 *	FULL IMPLEMENTATION FEATURES.	C129 3A 02 C8	#J50 VDAD	MOV L,A	INTO 'L'
C640	#176 *		C12C 05	#J51	LDA BOT	GET TEXT OFFSET
C640	#177 VDMOT	PUSH H	C12D 0F	#J52	L	ADD IT TO THE LINE POSITION
C640	#178 VDMOT	PUSH D	C12E 0F	#J53	RHC	TIMES TWO
C640	#179	PUSH B	C130 B6 03	#J54	RHC	MARLS FOUR
C640	#180	PUSH PSM	C132 57	#J55	ANI J	MOD THREE FOR LATER
C640	#181	MOV A,B	C133 3E CC	#J56	MOV D,A	
C640	#182	LXI H,TBL	C135 82	#J57	ANI A,<VDMEM	LOW SCREEN OFFSET
C640	#183	CALL TSRCH	C136 67	#J58	ADD	D
C640	#184		C137 70	#J59	MOV H,A	NUM H IS DONE
C640	#185 GOBACK	CALL VDADD	C138 B6 C8	#J60	ANI SCURH	TWIST L'S ARM
C640	#186	MOV A,M	C13A B1	#J61	ADD C	
C640	#187 OKI	98H	C13B 6F	#J62	MOV L,A	
C640	#188	MOV M,A	C13C 09	#J63	RET	
C640	#189 GOBK	POP PSM	C13D	#J64 *		H & L ARE NOW PERVERTED
C640	#190	POP B	C13D	#J65 *	ROUTING TO REMOVE CURSOR	
C640	#191	POP D	C13D	#J66 *		
C640	#192	POP H	C13D	#J67 *		
C640	#193	RET	C13D	#J68 *		
C640	#194 *		C13D	#J69 CRLM	CALL VDADD	GET CURRENT SCREEN ADDRESS
C640	#195 *		C13D	#J70	MOV A,M	
C640	#196 TSRCH	MOV A,M	C13D 7F	#J71	ANI TBL	STRIP OFF THE CURSOR
C640	#197	ORH A	C143 77	#J72	REI	
C640	#198	JZ CHAR	C144 C9	#J73 *		
C640	#199	CMP B	C145	#J74 *	ROUTINE TO BACKSPACE	
C640	#200	INX H	C145	#J75 *		
C640	#201	JNZ NEXT	C145 C0 00 C1	#J76 PHACK	CALL PLEFF	
C640	#202	PUSH H	C148 C0 21 C1	#J77	CALL VDADD	GET SCREEN ADDRESS
C640	#203	CALL CRLM	C148 36 20	#J78	AVI M,	PUT A BLANK THERE
C640	#204	POP H	C14C C9	#J79	RET	
C640	#205 *		C14E	#J80 *		
C640	#206 *		C14E	#J81 *	ROUTINE TO PROCESS A CARRIAGE RETURN	
C640	#207 *		C14E	#J82 *		
C640	#208 *	THIS ROUTINE DISPATCHES TO THE ADDRESS POINTED TO	C14E C0 E3 C8	#J83 PCR	CALL CLINE	CLEAR FROM CURRENT CURSOR TO END OF LINE
C640	#209 *	BY THE HL REGISTER PAIR. THE RETURN ADDRESS IS THE	C151 AF	#J84	XRA A	HAVING IT
C640	#210 *	LAST ENTRY ON THE STACK.	C152 C3 13 C1	#J85	JMP PCUR	AND STORE THE NEW VALUE
C640	#211 DISPT	MOV A,M	C155	#J86 *	ROUTINE TO PROCESS LINEFEED	
C640	#212	INX H	C155	#J87 *		
C640	#213	MOV H,M	C155	#J88 *		
C640	#214	MOV L,A	C155 3A 01 C8	#J89 PLF	LDA LINE	GET LINE COUNT
C640	#215	PCHL	C158 FE 0F	#J90	CVI 15	ARE WE AT THE BOTTOM?
C640	#216 *		C15A 04 01 C1	#J91	JNC SC	
C640	#217 *		C15B C3 C1 C8	#J92	INR A	
C640	#218 NEXT	INX H	C161	#J93	JMP CUR	ONE MORE LINE UP
C640	#219	INX H	C161 AF	#J94 SC	XRA A	
C640	#220	JMP TSRCH	C162 C3 9C C8	#J95	JMP SHOL	
C640	#221 *		C165	#J96 *		
C640	#222 *		C165	#J97 *		
C640	#223 CHAR	MOV A,B	C165	#J98 *		
C640	#224	ORH A	C165	#J99 *		
C640	#225	RZ	C165	#J100 *		
C640	#226	CVI 7FH	C165	#J101 *		
C640	#227	RZ	C165	#J102 *		
C640	#228 *		C165	#J103 *		
C640	#229 *		C165	#J104 *		
C640	#230 *		C165	#J105 *		
C640	#231 UCHAK	CALL VDADD	C165 00	#J106	DB CLEAR	SCREEN
C640	#232	MOV A,B	C165 05 C8	#J107	DB PERSE	
C640	#233	ANI 7FH	C169 04 C1	#J108	DB UP	CURSOR
C640	#234	MOV M,A	C16A 9A	#J109	DB POP	
C640	#235	LDA NCHAR	C16C FA C8	#J110	DB PUSHN	
C640	#236	CVI 63	C16E 01	#J111	DB LEFT	
C640	#237	JC OR	C171 00 C1	#J112	DB PLEFF	
C640	#238	LDA LINE	C172 17 C1	#J113	DB RIGHT	
C640	#239	CVI 15	C174 0E	#J114	DB PH11	
C640	#240	JNZ OR	C175 F3 C8	#J115	DB HOME	
C640	#241 *		C177 00	#J116	DB PHONE	
C640	#242 *	END OF SCREEN...ROLL UP ONE LINE	C178 4E C1	#J117	DB CR	CARRIAGE RETURN
C640	#243 *		C17A 0A	#J118	DB LFL	LINE FLD
C640	#244 SCROLL	XRA A	C17B 55 C1	#J119	DB PLF	BACK SPACE
C640	#245	STA A	C17C 5F	#J120	DB SACKS	BACK SPAC
C640	#246 SHUL	MOV C,A	C17E 45 C1	#J121	DB SACK	MODE KEY
C640	#247	CALL VDAD	C180 80 C1	#J122	DB CONNJ	END OF TABLE
C640	#248	XRA A	C181 04 C1	#J123 *		
C640	#249	LDA BOT	C183 00 C1	#J124 *		
C640	#250	INR A	C184	#J125 *	OUTPUT DEVICE TABLE	
C640	#251	ANI 0FH	C184	#J126 *		
C640	#252	JMP ERASJ	C184 4C C8	#J127 UFAB	DB VDADD	DISPLAY DRIVER
C640	#253 *		C186 4E C8	#J128	DB SEROT	SERIAL OUTPUT
C640	#254 *	INCREMENT LINE COUNTER IF NECESSARY	C188 0A C1	#J129	DB ERROT	ERROR HANDLER (FOR CONSUL)
C640	#255 *		C18A AD C1	#J130	DB ERROT	ERROR HANDLER
C640	#256 *		C18C	#J131 *	INPUT DEVICE TABLE	
C640	#257 JK	LDA NCHAR	C18C	#J132 *		
C640	#258	INP A	C18C 27 C8	#J133	DB ITAB	
C640	#259	STA NCHAR	C18E 36 C1	#J134	DB AD C1	
C640	#260	CVI 64	C190 AD C1	#J135	DB AD C1	
C640	#261	XRA A	C192 AD C1	#J136 *		
C640	#262	NCAR	C194	#J137 *		
C640	#263	STA LINE	C194	#J138 *		
C640	#264	LDA LINE	C194	#J139 *		
C640	#265	INR A	C194	#J140 *		
C640	#266	ANI 0FH	C194	#J141 *		
C640	#267	STA LINE	C194	#J142 *		
C640	#268	RET	C194	#J143 *		
C640	#269 *		C194	#J144 *		
C640	#270 *	ERASE SCREEN	C194	#J145 *		
C640	#271 *		C194 54 45	#J146	DB COMTAB	ASC "EL"
C640	#272 PERSE	LXI H,<VDMEM	C196 70 C2	#J147	DB TERM	
C640	#273	INX M,<BHH+	C198 44 55	#J148	DB DU	
C640	#274 *		C19A A1 C4	#J149	DB BUMP	
C640	#275 ERAS1	INX H	C19C 45 46	#J150	DB EN	
C640	#276	MOV A,H	C19E 07 C3	#J151	DB ENTER	
C640	#277	CVI 0DH	C1A0 45 58	#J152	DB EX	
C640	#278	JNC ERAS2	C1A2 35 C3	#J153	DB EXEC	
C640	#279	AVI M,	C1A4 54 C4	#J154	DB TUD	
C640	#280	JMP ERAS1	C1A6 39 C3	#J155	DB TUDAD	
C640	#281		C1A8 42 41	#J156	ASC BA	SPECIAL COMMAND TO EXECUTE 0
C640	#282 ERAS2	XRA A	C1AA 00 00	#J157	DB 0	
C640	#283	STA LINE	C1AC 00	#J158	DB 0	END OF TABLE MARK
C640	#284	LDA NCHAR	C1AD	#J159 *		
C640	#285 *		C1AD	#J160 *		
C640	#286 ERAS3	OUT DSTAT	C1AD	#J161 *	CONSOL PORT ERROR HANDLER	
C640	#287	STA BOT	C1AD AF	#J162	DB ERROT	XRA A
C640	#288	RET	C1AE 32 04 C8	#J163	DB STA	IPOINT
C640	#289 *		C1B1 03 03 C8	#J164	DB SPOINT	DEFAULT TO SCREEN
C640	#290 *		C1B4	#J165 *		
C640	#291 CLINE	CALL VDADD	C1B4	#J166 *		
C640	#292	LDA NCHAR	C1B4	#J167 *		
C640	#293 CLINI	CVI 64	C1B4	#J168 *		
C640	#294	RHC	C1B4	#J169 *		
C640	#295	AVI M,	C1B4	#J170 *		
C640	#296	INX H	C1B4	#J171 *		
C640	#297	AVI A	C1B4	#J172 *		
C640	#298	JMP CLINI	C1B4	#J173 *		
C640	#299 *		C1B4	#J174 *		
C640	#300 *	HOME CURSOR	C1B4 31 00 C8	#J175 CONRD	LXI SP,SYSTP	SET STACK POINTER
C640	#301 *		C1B7 C0 12 C2	#J176	CALL PROMT	PROMT ON SCREEN
C640	#302 PHORE	XRA A	C1BA C0 C1	#J177	CALL GCLIN	GET COMMAND LINE
C640	#303	STA NCHAR	C1BC C0 E1 C1	#J178	CALL COPRC	PROCESS THE LINE
C640	#304	JMP CUR	C1C4 C3 04 C1	#J179	JMP CONRD	OVER AND OVER
C640	#305 *		C1C3	#J180 *		
C640	#306 *	MOVE CURSOR DOWN ONE LINE	C1C3	#J181 *		
C640	#307 *		C1C3	#J182 *		
C640	#308	LDA LINE	C1C3	#J183 *		
C640	#309	CVI 15	C1C3	#J184 *		
C640	#310	RZ	C1C3	#J185 *		
C640	#311	INR A	C1C3	#J186 *		
C640	#312	JMP CUR	C1C3	#J187 *		
C640	#313 *		C1C3	#J188 *		
C640	#314 *	ROUTINE TO MOVE THE CURSOR UP ONE LINE	C1C3	#J189 *		
C640	#315 *		C1C3 C0 28 C8	#J190	CALL KREAD	READ KEYBOARD
C640	#316 PUP	LDA LINE	C1C6 FE 20	#J191	CVI 20H	
C640	#317	DRA A	C1C8 47	#J192	MOV J,A	
C640	#318	INX H	C1CA DA 02 C1	#J193	JC	PROCESS CONTROL CHARACTER
C640	#319	DCR A	C1CC 00 4B C8	#J194	CALL VDMOT	
C640	#320	JMP CUR	C1CF C3 C3 C1	#J195	JMP GCLIN	
C640	#321 *		C1D0	#J196 *		
C640	#322 *	MOVE CURSOR LEFT ONE POSITION	C1D2	#J197 *	PROCESS CONTROL KEYS	
C640	#323 *		C1D2	#J198		
C640	#324 PLEFF	LDA NCHAR	C1D2 FE 00	#J199	DB PHORE	CP1 CR
C640	#325	ORA A	C1D4 CA 00 C1	#J200	JZ	CP1 CRPC
C640	#326	RZ	C1D7 FE 0A	#J201	CP1 LF	
C640	#327	DCR A	C1D9 C8	#J202	RZ	IF SO GO PROCESS
C640	#328 PCUR	STA NCHAR	C1DA C3 C3 C1	#J203	JMP GCLIN	NO CONTROL CHARS TO SCREEN
C640	#329	RET	C1DD	#J204		
C640	#330 *		C1DD	#J205		
C640	#331 *	CURSOR RIGHT ONE POSITION	C1DD C0 E3 C8	#J206	CALL CLINE	CLEAR REMAINING LINE
C640	#332 *		C1E4 C9	#J207	RET	NOW PROCESS
C640	#333 PHIT	LDA NCHAR	C1E1	#J208 *		
C640	#334	CVI 63	C1E1	#J209 *		
C640	#335		C1E1	#J210 *		
C640	#336		C1E1	#J211 *		
C640	#337		C1E1	#J212 *		
C640	#338		C1E1	#J213 *		
C640	#339		C1E1	#J214 *		
C640	#340		C1E1	#J215 *		
C640	#341		C1E1	#J216 *		
C640	#342		C1E1	#J217 *		
C640	#343		C1E1	#J218 *		
C640	#344		C1E1	#J219 *		
C640	#345		C1E1	#J220 *		
C640	#346		C1E1	#J221 *		
C640	#347		C1E1	#J222 *		
C640	#348		C1E1	#J223 *		
C640	#349		C1E1	#J224 *		
C640	#350		C1E1	#J225 *		
C640	#351		C1E1	#J226 *		
C640	#352		C1E1	#J227 *		
C640	#353		C1E1	#J228 *		
C640	#354		C1E1	#J229 *		
C640	#355		C1E1	#J230 *		
C640	#356		C1E1	#J231 *		
C640	#357		C1E1	#J232 *		
C640	#358		C1E1	#J233 *		
C640	#359		C1E1	#J234 *		
C640	#360		C1E1	#J235 *		
C640	#361		C1E1	#J236 *		
C640	#362		C1E1	#J237 *		
C640	#363		C1E1	#J238 *		
C640	#364		C1E1	#J239 *		
C640	#365		C1E1	#J240 *		

SOFTWARE SECTION

MICROCOMPUTER DEVELOPMENT SOFTWARE

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C161 C0 30 C1 0512 *
C161 0E 01 0513 COPRC CALL CREN REMOVE THE CURSOR
C161 0E 25 C1 0514 CALL VDDA2 SET FOR CHARACTER POSITION
C161 0E 25 C1 0515 CALL VDDA2 SET SCREEN ADDRESS
C161 0E 32 C2 0516 XCHG SCAN PAST BLANKS
C161 0E 32 C2 0517 CALL SCHR NO COMMAND?
C161 0E 32 C2 0518 JZ ERR1 HL HAS FIRST CHR
C161 0E 32 C2 0519 XCHG HL, COMTAS POINT TO COMMAND TABLE
C161 0E 32 C2 0520 LRI D, COMTAS
C161 0E 32 C2 0521 *
C161 0E 32 C2 0522 * THIS ROUTINE SEARCHES THROUGH A TABLE, POINTED TO
C161 0E 32 C2 0523 * BY 'DE', FOR A DOUBLE CHARACTER MATCH OF THE 'HL'
C161 0E 32 C2 0524 * MEMORY CONTENT. IF NO MATCH IS FOUND THE SCAN ENDS
C161 0E 32 C2 0525 * BY PLACING A QUESTION MARK WITHIN THE SEARCH STRING.
C161 0E 32 C2 0526 *
C161 0E 32 C2 0527 FDOCM LDX D
C161 0E 32 C2 0528 ORA A TEST FOR TABLE END
C161 0E 32 C2 0529 JZ ERR2 NO FOUND... COMMAND ERROR
C161 0E 32 C2 0530 PUSH H SAVE START OF SCAN ADDRESS
C161 0E 32 C2 0531 CNP H HL HAS FIRST CHR
C161 0E 32 C2 0532 INX D TEST FIRST CHR
C161 0E 32 C2 0533 JNZ NCOM
C161 0E 32 C2 0534 *
C161 0E 32 C2 0535 INX H
C161 0E 32 C2 0536 LDX D
C161 0E 32 C2 0537 CNP H NO SECOND CHARACTER
C161 0E 32 C2 0538 JNZ NCOM GOODNESS
C161 0E 32 C2 0539 *
C161 0E 32 C2 0540 POP B CLEAR THE STACK
C161 0E 32 C2 0541 XCHG DE HAS SCAN ADDRESS
C161 0E 32 C2 0542 INX H HL HAS COMMAND ADDRESS
C161 0E 32 C2 0543 JNP DISPT DISPATCH TO IT
C161 0E 32 C2 0544 *
C161 0E 32 C2 0545 *
C161 0E 32 C2 0546 NCOM INX D GO TO NEXT ENTRY
C161 0E 32 C2 0547 INX D
C161 0E 32 C2 0548 INX D
C161 0E 32 C2 0549 POP H GET BACK ORIGINAL ADDRESS
C161 0E 32 C2 0550 JNP FDOCM CONTINUE SEARCH
C161 0E 32 C2 0551 *
C161 0E 32 C2 0552 *
C161 0E 32 C2 0553 * OUTPUT A CHLF FOLLOWED BY A PROMPT
C161 0E 32 C2 0554 * (WITH CONSOL ALL OPERATIONS ARE ON THE SCREEN)
C161 0E 32 C2 0555 *
C161 0E 32 C2 0556 PROMPT CALL CHLF
C161 0E 32 C2 0557 MVI D, ' ' THE PROMPT
C161 0E 32 C2 0558 JNP VDMOT PUT IT ON THE SCREEN
C161 0E 32 C2 0559 *
C161 0E 32 C2 0560 CHLF MVI B, LF LINE FEED
C161 0E 32 C2 0561 CALL VDMOT CARRIAGE RETURN
C161 0E 32 C2 0562 MVI B, CH
C161 0E 32 C2 0563 JNP VDMOT PUT IT OUT AND RETURN
C161 0E 32 C2 0564 *
C161 0E 32 C2 0565 *
C161 0E 32 C2 0566 * SCAN OVER UP TO 12 CHARACTERS LOOKING FOR A BLANK
C161 0E 32 C2 0567 *
C161 0E 32 C2 0568 SBK MVI C, 12 MAXIMUM COMMAND STRING
C161 0E 32 C2 0569 SBK LDX D
C161 0E 32 C2 0570 CPI BLANK
C161 0E 32 C2 0571 JZ SCHR GOT A BLANK NOW SCAN PAST IT
C161 0E 32 C2 0572 INX H
C161 0E 32 C2 0573 DCR C NO MORE THAN TWELVE
C161 0E 32 C2 0574 JNZ SBK1 GO BACK WITH ZERO FLAG SET
C161 0E 32 C2 0575 HLT
C161 0E 32 C2 0576 *
C161 0E 32 C2 0577 *
C161 0E 32 C2 0578 * SCAN PAST UP TO 16 BLANK POSITIONS LOOKING FOR
C161 0E 32 C2 0579 * A NON BLANK CHARACTER.
C161 0E 32 C2 0580 *
C161 0E 32 C2 0581 SCHR MVI C, 16 SCAN TO FIRST NON BLANK CHR WITHIN 16
C161 0E 32 C2 0582 SBK LDX D GET NEXT CHARACTER
C161 0E 32 C2 0583 CPI SPACE
C161 0E 32 C2 0584 RNZ
C161 0E 32 C2 0585 INX D WE'VE PAST THEM
C161 0E 32 C2 0586 DCR C NEXT SCAN ADDRESS
C161 0E 32 C2 0587 RZ COMMAND ERROR
C161 0E 32 C2 0588 JNP SCHR1 KEEP LOOPING
C161 0E 32 C2 0589 *
C161 0E 32 C2 0590 * THIS ROUTINE SCANS OVER CHARACTERS, PAST BLANKS AND
C161 0E 32 C2 0591 * CONVERTS THE FOLLOWING ADDRESS TO HEX. ERRORS RETURN TO
C161 0E 32 C2 0592 * THE ERROR HANDLER.
C161 0E 32 C2 0593 *
C161 0E 32 C2 0594 SCOV CALL SBK
C161 0E 32 C2 0595 JZ ERR1
C161 0E 32 C2 0596 *
C161 0E 32 C2 0597 * THIS ROUTINE CONVERTS ASCII DIGITS INTO BINARY FOLLOWING
C161 0E 32 C2 0598 * A STANDARD HEX CONVERSION. THE SCAN STOPS WHEN AN ASCII
C161 0E 32 C2 0599 * SPACE IS ENCOUNTERED. PARAMETER ERRORS REPLACE THE ERROR
C161 0E 32 C2 0600 * CHARACTER ON THE SCREEN WITH A QUESTION MARK.
C161 0E 32 C2 0601 *
C161 0E 32 C2 0602 JHEX LRI H, 0 CLEAR H & L
C161 0E 32 C2 0603 SHL LDX D GET CHARACTER
C161 0E 32 C2 0604 CPI 20H IS IT A SPACE?
C161 0E 32 C2 0605 RZ IF SO
C161 0E 32 C2 0606 *
C161 0E 32 C2 0607 NCOMV DAD H MAKE ROOM FOR THE NEW ONE
C161 0E 32 C2 0608 DAD H
C161 0E 32 C2 0609 DCR H
C161 0E 32 C2 0610 *
C161 0E 32 C2 0611 CALL HCONV DO THE CONVERSION
C161 0E 32 C2 0612 JNC ERR1 NOT VALID HEXIDECIMAL VALUE
C161 0E 32 C2 0613 INX L
C161 0E 32 C2 0614 MOV B, A MOVE IT IN
C161 0E 32 C2 0615 INX D BUMP THE POINTER
C161 0E 32 C2 0616 JNP SHL1
C161 0E 32 C2 0617 *
C161 0E 32 C2 0618 HCONV SUI 48 REMOVE ASCII BIAS
C161 0E 32 C2 0619 CPI 10
C161 0E 32 C2 0620 JC IF LESS THAN 9
C161 0E 32 C2 0621 SUI 7 IF A LETTER?
C161 0E 32 C2 0622 CPI 10H
C161 0E 32 C2 0623 RST WITH TEST IN HAND
C161 0E 32 C2 0624 *
C161 0E 32 C2 0625 *
C161 0E 32 C2 0626 * SYSTEM START UP, CLEAR PART OF RAM AND SET STACK
C161 0E 32 C2 0627 * POINTER, TAILING THROUGH TO TERMINAL ROUTE.
C161 0E 32 C2 0628 *
C161 0E 32 C2 0629 *
C161 0E 32 C2 0630 STRA RSA A
C161 0E 32 C2 0631 MOV C, A WE CLEAR THE FIRST 256 BYTES
C161 0E 32 C2 0632 LRI H, SYSRAM POINT TO SYSTEM RAM
C161 0E 32 C2 0633 CLERA MOV A, A
C161 0E 32 C2 0634 INX H
C161 0E 32 C2 0635 INX C
C161 0E 32 C2 0636 JNZ CLERA CLEAR FIRST 256 BYTES
C161 0E 32 C2 0637 *
C161 0E 32 C2 0638 *
C161 0E 32 C2 0639 *
C161 0E 32 C2 0640 *
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C161 0E 32 C2 0844 *
C161 0E 32 C2 0845 *
C161 0E 32 C2 0846 *
C161 0E 32 C2 0847 *
C161 0E 32 C2 0848 *
C161 0E 32 C2 0849 *
C161 0E 32 C2 0850 *
C161 0E 32 C2 0851 *
C161 0E 32 C2 0852 *
C161 0E 32 C2 0853 *
C161 0E 32 C2 0854 *
C161 0E 32 C2 0855 *
C161 0E 32 C2 0856 *
C161 0E 32 C2 0857 *
C161 0E 32 C2 0858 *
C161 0E 32 C2 0859 *
C161 0E 32 C2 0860 *
C161 0E 32 C2 0861 *
C161 0E 32 C2 0862 *
C161 0E 32 C2 0863 *
C161 0E 32 C2 0864 *
C161 0E 32 C2 0865 *
C161 0E 32 C2 0866 *
C161 0E 32 C2 0867 *
C161 0E 32 C2 0868 *
C161 0E 32 C2 0869 *
C161 0E 32 C2 0870 *
C161 0E 32 C2 0871 *
C161 0E 32 C2 0872 *
C161 0E 32 C2 0873 *
C161 0E 32 C2 0874 *
C161 0E 32 C2 0875 *
C161 0E 32 C2 0876 *
C161 0E 32 C2 0877 *
C161 0E 32 C2 0878 *
C161 0E 32 C2 0879 *
C161 0E 32 C2 0880 *
C161 0E 32 C2 0881 *
C161 0E 32 C2 0882 *
C161 0E 32 C2 0883 *
C161 0E 32 C2 0884 *
C161 0E 32 C2 0885 *
C161 0E 32 C2 0886 *
C161 0E 32 C2 0887 *
C161 0E 32 C2 0888 *
C161 0E 32 C2 0889 *
C161 0E 32 C2 0890 *
C161 0E 32 C2 0891 *
C161 0E 32 C2 0892 *
C161 0E 32 C2 0893 *
C161 0E 32 C2 0894 *
C161 0E 32 C2 0895 *
C161 0E 32 C2 0896 *
C161 0E 32 C2 0897 *
C161 0E 32 C2 0898 *
C161 0E 32 C2 0899 *
C161 0E 32 C2 0900 *
C161 0E 32 C2 0901 *
C161 0E 32 C2 0902 *
C161 0E 32 C2 0903 *
C161 0E 32 C2 0904 *
C161 0E 32 C2 0905 *
C161 0E 32 C2 0906 *
C161 0E 32 C2 0907 *
C161 0E 32 C2 0908 *
C161 0E 32 C2 0909 *
C161 0E 32 C2 0910 *
C161 0E 32 C2 0911 *
C161 0E 32 C2 0912 *
C161 0E 32 C2 0913 *
C161 0E 32 C2 0914 *
C161 0E 32 C2 0915 *
C161 0E 32 C2 0916 *
C161 0E 32 C2 0917 *
C161 0E 32 C2 0918 *
C161 0E 32 C2 0919 *
C161 0E 32 C2 0920 *
C161 0E 32 C2 0921 *
C161 0E 32 C2 0922 *
C161 0E 32 C2 0923 *
C161 0E 32 C2 0924 *
C161 0E 32 C2 0925 *
C161 0E 32 C2 0926 *
C161 0E 32 C2 0927 *
C161 0E 32 C2 0928 *
C161 0E 32 C2 0929 *
C161 0E 32 C2 0930 *
C161 0E 32 C2 0931 *
C161 0E 32 C2 0932 *
C161 0E 32 C2 0933 *
C161 0E 32 C2 0934 *
C161 0E 32 C2 0935 *
C161 0E 32 C2 0936 *
C161 0E 32 C2 0937 *
C161 0E 32 C2 0938 *
C161 0E 32 C2 0939 *
C161 0E 32 C2 0940 *
C161 0E 32 C2 0941 *
C161 0E 32 C2 0942 *
C161 0E 32 C2 0943 *
C161 0E 32 C2 0944 *
C161 0E 32 C2 0945 *
C161 0E 32 C2 0946 *
C161 0E 32 C2 0947 *
C161 0E 32 C2 0948 *
C161 0E 32 C2 0949 *
C161 0E 32 C2 0950 *
C161 0E 32 C2 0951 *
C161 0E 32 C2 0952 *
C161 0E 32 C2 0953 *
C161 0E 32 C2 0954 *
C161 0E 32 C2 0955 *
C161 0E 32 C2 0956 *
C161 0E 32 C2 0957 *
C161 0E 32 C2 0958 *
C161 0E 32 C2 0959 *
C161 0E 32 C2 0960 *
C161 0E 32 C2 0961 *
C161 0E 32 C2 0962 *
C161 0E 32 C2 0963 *
C161 0E 32 C2 0964 *
C161 0E 32 C2 0965 *
C161 0E 32 C2 0966 *
C161 0E 32 C2 0967 *
C161 0E 32 C2 0968 *
C161 0E 32 C2 0969 *
C161 0E 32 C2 0970 *
C161 0E 32 C2 0971 *
C161 0E 32 C2 0972 *
C161 0E 32 C2 0973 *
C161 0E 32 C2 0974 *
C161 0E 32 C2 0975 *
C161 0E 32 C2 0976 *
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C161 0E 32 C2 0978 *
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C161 0E 32 C2 0981 *
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C161 0E 32 C2 0984 *
C161 0E 32 C2 0985 *
C161 0E 32 C2 0986 *
C161 0E 32 C2 0987 *
C161 0E 32 C2 0988 *
C161 0E 32 C2 0989 *
C161 0E 32 C2 0990 *
C161 0E 32 C2 0991 *
C161 0E 32 C2 0992 *
C161 0E 32 C2 0993 *
C161 0E 32 C2 0994 *
C161 0E 32 C2 0995 *
C161 0E 32 C2 0996 *
C161 0E 32 C2 0997 *
C161 0E 32 C2 0998 *
C161 0E 32 C2 0999 *
C161 0E 32 C2 1000 *

```


C300 C2 73 C3	0854	JNZ	KIBYF	STILL MORE IF NOT ZERO
C300	0855	*		
C300 CD C1 C3	0856	CALL	CRCKC	CHECK CRC AND FALL THROUGH TO ERROR
C303 CA 61 C3	0857	JMP	LOLOOP	TEST OK
C308	0858	*		
C306 06 07	0859	LDHR	MVI	0,"G"=40H
C306 CA 08 C4	0859	CALL	VLENR	BELL CHARACTER
C303 04 C1 C3	0861	JMP	COMND	PUT IT ON THE SCREEN
C306	0862	*		
C306	0863	*		
C306	0864	*		
C306	0865	*		
C306	0866	ERHL	XORG	CONSOLE ERROR HANDLER
C306 3F 3F	0867	BRK2	MVI	" , ?"
C303 C3 04 C1	0868	*	JMP	COMND
C304	0869	*		
C304	0870	*		
C304 06 0A	0872	RHADD	MVI	B,10
C306 0A 0A	0873	RHEAL	IN	SIAP1
C306 06 0A	0874	ANI	TOR	FIND 10 NULLS
C306 CA 9A C3	0875	RHALL	JZ	GET A BYTE
C306 0A 0A	0876	IN	TDATA	
C307 07	0877	JWA	A	IGNORE ERROR CONDITIONS
C306 C2 94 C3	0878	JZ	RHADD	ZERO?
C307 07	0879	DCR	B	
C304 C2 96 C3	0880	JNZ	RHALL	LOOP UNTIL 10 IN A ROW
C307	0881	*		
C307	0882	*		
C307	0883	*		
C307 C0 C6 C3	0884	SUHL	CALL	TAPIN
C304 30	0885	DCR	A	
C306 C2 A7 C3	0886	JNZ	SUHL	WAIT FOR A '1'
C306	0887	*		
C306	0888	*		
C306	0889	*		
C306	0890	*		
C306 21 03 C8	0890	LXI	H,THRAD	POINT TO BUFFER
C301 01 00 10	0891	LXI	B,BLENR+255	LENGTH OF HEADER IN "B",C8
C306	0892	*		
C304 C0 C6 C3	0893	RHDI	CALL	TAPIN
C307 77	0894	MOV	M,A	GET BYTE
C306 05	0895	INX	H	STORE IT
C306 A9	0896	XRA	C	INCREMENT ADDRESS
C30A 2F	0897	CMA	*	NO CALCULATE THE CRC
C306 2F	0898	SUB	C	INSIDE OUT AND UPSIDE DOWN
C306 05	0899	NOV	C,A	SQUEEZE IT
C306 C2 04 C3	0900	DCR	B	AWSAVE AGAIN
C306	0901	JNZ	HIED1	WHOLE HEADER YES?
C301	0902	*		
C301	0903	*		
C301	0904	*		
C301	0905	*		
C301	0906	*		
C306 C0 C6 C3	0907	CHCK	CALL	TAPIN
C304 09	0908	CRP	C	GET CRC BYTE
C305 C9	0909	RET		COMPARE IT WITH CALCULATED
C306	0910	*		
C306	0911	*		
C306	0912	*		
C306	0913	*		
C306	0914	*		
C306	0915	*		
C306	0916	*		
C306 0A 0A	0917	TAPIN	IN	SIAP1
C306 06 0A	0918	ANI	TOR	CHECK STATUS
C306 C2 07 C3	0919	JNZ	TDATA	
C306 0A 0A	0920	IN	KDATA	ONE IS AVAILABLE
C306 0A 0A	0921	CPI	NOEL	CHECK FOR MODE WHILE WE'RE WAITING
C306 CA 0A C1	0922	JZ	COMND	
C306 C2 C6 C3	0923	JMP	TAPIN	MODE WAS GIVEN...ABOUT OPERATION
C307	0924	*		
C307 0A 0A	0925	TREDF	IN	NOT MODE...SIAP1 IN LOOP
C306 06 18	0926	ANI	TFL+TUL	
C306 C2 06 C3	0927	TOR		DATA ERROR?
C306 0A 0A	0928	IN	TDATA	IF FRAMING OR OVERRUN ERROR
C306 C9	0929	RJZ		GET THE DATA
C301	0930	*		
C301	0931	*		
C301	0932	*		
C301 01 FF FF	0933	BLR	LXI	B,-1
C304 09	0934	DAI	B	COMPLEMENT HL
C305 23	0935	INX	HTWO'S
C306 05	0936	MOV	M,M	B.L
C307 21 00 0A	0937	LXI	H,0	TELL DE WE'RE DONE
C30A C3 76 C3	0938	JAP	RDEK	ONWARD TO THE END
C306	0939	*		
C306	0940	*		
C306	0941	*		
C306 0A AF	0942	TUFF	XRA	A
C306 C3 0A	0943	OUT	SIAP1	GIVE COMMAND
C306 C9	0944	RET		AND URIND TO A SLOW STOP
C306	0945	*		
C306	0946	*		
C301 11 00 00	0947	DELY	LXI	D,0
C304 18	0948	DELY	MOV	D
C305 7A	0949	AND	A,D	START LOW

C000	1020 *			
C001	1029 *			
C002	1030 *			
C003	1031 *			CONSUL PARAMETER AREA
C004	1032 ACNAR	DS	1	CURRENT CHARACTER POSITION
C005	1033 LINE	DS	1	CURRENT LINE POSITION
C006	1034 BOL	DS	1	BEGINNING OF TEXT DISPLACEMENT
C007	1035 OUPUT	DS	1	OUTPUT PORT
C008	1036 INPUT	DS	1	INPUT PORT
C009	1037 *			
C009	1038 *			
C009	1039 *			
C009	1040 THEAD	DS	5	NAME
C009	1041	DS	1	THIS BYTE MUST BE ZERO
C009	1042 HTYPE	DS	1	TYPE
C009	1043 BLOCK	DS	2	BLOCK SIZE
C009	1044 LOADH	DS	2	LOAD ADDRESS
C010	1045 XLOAD	DS	2	AUTO EXECUTE ADDRESS
C012	1046 MARK	DS	3	SPARE
C013	1047 *			
C015	1048 BLLEN	EQW	5-THEAD	LENGTH OF HEADER
C015	1049 *			
C015	1050 *			

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CIRCLE INQUIRY NO. 37

LLL 8080 Basic Interpreter Program

PART II

By John Dickenson and Jerry Barber

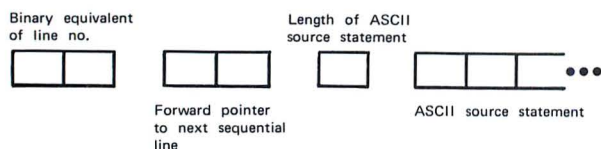
INTRODUCTION

This article is part #2 of a series of four articles covering the LLL 8080 BASIC Interpreter program released to the public domain by Lawrence Livermore Laboratories. This article covers the description of the BASIC Interpreter and includes the assembly listing of the LLL 8080 BASIC Interpreter program.

DESCRIPTION OF BASIC INTERPRETER

Following is a brief description of the BASIC interpreter. Hopefully, with this description, it will not be a major project to modify the BASIC to satisfy the reader's specific needs.

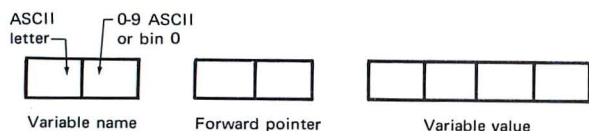
Formats — Source statements are stripped of blanks on input (character strings enclosed in " "s are an exception) and stored as is in memory, using the following format:



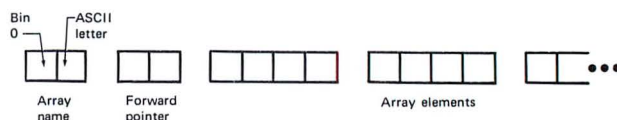
The forward pointer links statements by ascending line numbers. The last line's forward pointer (supposedly an end statement) has value 177777₈ to indicate end of the list.

The symbol table is built up at run time and begins after the most recently entered source statement (the variable STSPAC points to where the symbol table will start). Symbol table entries are shown below:

SCALAR-VARIABLE FORMAT



ARRAY-VARIABLE FORMAT



Subroutines — Following is a list of potentially useful subroutines, with a brief description of each subroutine:

- ALPHA** — Value pointed to by H and L is tested to see if it is an ASCII letter.
CY = 1 => Yes
CY = 0 => No
- NUMB** — Same as above but tests for a decimal number (ASCII 0-9).
- CHAR2** — Inputs a character from the teletype to a register.
- CHAR5** — Same as above for HSR (High Speed Paper Tape Reader).
- CHK1** — Checks to see if HL are equal to 177777₈ (-1).
CY = 1 => Yes
CY = 0 => No.
- CONV (CVRT)** — One of the floating-point routines. Converts floating-point number to a character string. Output is padded to the output buffer.
- COPDH** — Copies floating-point number pointed to by D, E to location pointed to by H, L; uses copy.
- COPY** — One of the floating-point routines. Copies floating-point value pointed to by A, L to location pointed to by H, C.
- CUB** — Converts the integer-character string pointed to by H, L to its binary equivalent. Value returns in D, E registers.
- DCOMP** — Double-byte comparison routine. Compares value in CB to the value in ED.

	$Z = 1 \Rightarrow CB = ED$ $CY = 1 \Rightarrow CB > ED$ $CY = 0 \Rightarrow CB \leq ED$		
DFXL	— One of the floating-point routines. Used to float an unsigned integer H, L point to first of four bytes; integer is right justified in first three bytes.	NSRCH	— Routine to locate source line in memory passed binary value of line number in DE. Returns address of line in HL, $CY = 1 \Rightarrow$ not found.
EVAL	— Evaluates an expression the first element of which is pointed to by H, L and the length of which is in C. Used to evaluate expressions wherever they are legal in BASIC. C usually contains the length of the source statement line containing the expression.	OUTR	— Used by CONV (CURT) to pad output to output buffer.
FINPT	— One of the floating-point routines. Converts character string to floating-point number. The variable HLINP contains a pointer to the character string, and the variable CREG contains the length of line containing character string. Mode = 0 \Rightarrow data comes from teletype (i.e., only delimiters are g's). Mode = 1 \Rightarrow data comes from source statements.	PAD	— Pads characters to output buffer. A contains character; B contains number of pads.
FIX	— Fixes a floating-point number. DE points to number to be fixed. Error code 13 is given if number is too big to fix.	SYMSRT	— Checks a character string to see if it is a BASIC symbol. HL contains address pointing to 1st character of symbol, C contains length of line that contains symbol. A contains type of symbol sought. 0=command 1=keyword z=operator or delimiter 3=function Returns with 377 ₈ in a register if nothing found. Otherwise A contains symbol number in appropriate KDAT table. Thus, for symbol type 2, if a 4 is returned, the symbol found was the fourth one (starting with 0) in table KDAT3 (KDAT concatenated with 2 and 1 or A). CIS is updated, but HL is not.
FSYM	— Finds symbols in symbol table. BC contains symbol. Returns with HL pointing to symbol value. $CY = 1 \Rightarrow$ symbol was found. $CY = 0$ and a scalar \Rightarrow symbol not found, but inserted and initialized to 0. $CY = 0$ and an array \Rightarrow not found, no action taken: HL are meaningless.	TTYIW	— Inputs a line from teletype. Stores starting address at location pointed to by HL. Line edits. Returns length of line in A register (maximum line length is 72 characters).
LADD	— Floating-point add routine.	VALUE	— Called with HL pointing to A variable, constant, or function; C contains line length, returns with DE pointing to floating-point value. HL, C are updated.
LSUB	— Floating-point subtract routine.	VAR	— Called with HL pointing to character string, C has line length. Determines if character string is a variable. If so, returns with $CY = 1$, DE pointing to value (subscripts of arrays are evaluated, etc.). HL, C updated. If not, a variable returns $CY = 0$, HL, C untouched.
LOIU	— Floating-point divide routine.	WRIT	— Dumps contents of output buffer to teletype. Uses entry WRIT1 with D register equal to one to suppress CR/LF.
LMUL	— Floating-point multiply routine.	ZROL	— Part of floating-point subroutines. Writes a floating-point zero, starting at location pointed to by HL.
LMCM	— One of the floating-point routines. Compares two floating-point values, HL Point to first floating-point values and HB point to second floating-point value. $z = 1 \Rightarrow$ Equality $Cy = 1 \Rightarrow$ first < second (Note: compares absolute only, does not reference mantissa sign.)		
MCHK	— Waits for flag from port 3. Proper mask is sent in register B.		
MEMFUL	— Checks to see if memory is full. HL point to location of memory to be checked. Memory is considered full if it is within 50 ₁₀ locations of the current value of stack pointer.		
MULT	— Multiplies two two-byte binary numbers. HL point to last byte of four bytes. First two contain first number. Last two contain second number. Answer returns in BCDE.		

The preceding list contains those subroutines most likely to be used by someone modifying BASIC. If you plan on using one of the routines, you should examine it and its comments carefully.

Variables — Following is a list of interpreter variables, with a description of each variable:

MEMST — Assembly time variable. Contains the first available RAM location. This is where active variables start.

MEMEND — Assembly time variable. Contains the last available location in RAM.

SEND	— Has value 6, used with RST instruction to print characters via ODT.
OBUFF	— Output buffer, the first location contains the number of characters in the buffer + 1.
IBUF	— Input buffer, occupies same area as OBUFF.
STLINE	— Points to first source line to be executed. If no source, contains 177777 ₈ .
NLINE, NL2, NL4, NL6	— Contain address, binary-equivalent line number, forward pointer, and length of next input line.
KLINE, KL2, KL4, KL6	— Same as above, but used by a subroutine that inserts lines in sequential order (insert).
PLINE, PL2, PL4, PL6	— Subroutine insert to order statements sequentially.
KASE, LEN	— Temporary storage for command mode routines.
MULT1, MULT2	— Used to store binary values to be multiplied.
SBSAV	— Temporary storage for call-statement processor.
STSPAC	— Next available location in memory, symbol table starts here at run time.
LPNT	— Pointer to the current line at run time.
CPNT	— Pointer to current character in current line at run time.
KFPNT	— Point to next sequential line at run time.
FREG1, FREG2	— Two floating-point registers.
HLINP, CREG	— Temporary storage for HL and C registers for routine INP.
NXTSP	— Pointer to next available space of memory for symbol table.
GREG	— General register, in and out instructions are stored here and executed for get and put functions.
MODE	— Indicates to INP routine whether input data comes from source or teletype.
MESCR	— Temporary storage for call-statement processor. Points to next available space

after symbol table. Area after the symbol table is used to store intermediate results of expressions or constants passed to user subroutines.

VARAD — Temporary storage space for input-statement processor.

VEND — Assembly time variable. Indicates end of interpreter variable-storage area and where FWAM pointer is to go.

FWAM — First word of available memory pointer. This is where user source programs go.

Some of the above variables occupy the same area of memory. This is because some variables are used only in the command mode and others only at runtime. To conserve space, they share the same memory locations.

New BASIC Statements — To add additional statements to the BASIC, use the following procedure. First, insert the statement keyword in the data tables for subroutine SYMSRT. Then, insert the starting address of the statement processor in the interpreter JUMP table. Finally, the statement processor itself must be inserted.

The keyword must be entered in the table KDAT2. The first byte must be the keyword length and the next bytes hold the ASCII-coded keyword. The table must end with A 377₈. If the keyword is the Nth entry in the table, on return from SYMSRT, the A register will hold N-1 if the keyword is found.

The starting address of the statement processor must be inserted into table JTBL. The order of keywords in KDAT2 must correspond with statement processor addresses in JTBL since, on return from SYMSRT, the A register times two is used as offset in JTBL to determine processor address.

The statement processor must be placed somewhere in memory. Generally, the first thing done in the statement processors is to load the pointer to the statement (LHLD CPNT) and increment past the keyword (since HL is not updated by SYMSRT). On entry, C contains the number of characters in the line minus those checked by SYMSRT. The end of the processor should be a "JMPIEND" instruction.

New Functions — New functions must be added to SYSSRT Data Table KDAT4 in the same manner as for key words. The function itself must be placed in subroutine "VALUE." Presently, the only function in VALUE is GET.

Message Lines — The following description tells how to incorporate messages into BASIC output routines. Currently, to output a message to the teletype, the user executes an LXI H,ODATA, then a call to FORMK where K is an integer indicating which message is wanted (i.e., K=z indicates "TURN ON PUNCH"). FORM pads the message into the output buffer. Then A "CALL WRIT" writes the contents of the buffer.

Suppose the message "POTATO BASIC" is to be added. Preceding the form 9 instruction, we will insert "FOR10: INR L." At the end of the ODATA table, we

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158E	21	13	10	ROUTINE TO OUTPUT ERROR MSG. TO USER. REG A CONTAINS BCD ERROR NUMBER, HL LOADED WITH VALUE OF KLINE.	16C0	5F	00	MOV	E,A		
15C1	E5			ERROR: LXI H,M1A	16C1	19		MVI	D,0		
15C2	21	5A	14	PUSH H	1601	23		DAD	D		:PNT. TO PROPER PROC.
15C3	E5			INX H	1602	23		MOV	A,M		:ADD. IN JUMP TABLE
15C4	06	01		PUSH H	1603	66		INX	H		:GET PROC. ADD.
15C5	57			MOV D,A	1604	66		MOV	H,M		
15C6	CD	46	14	CALL FORM3	1605	6F		MOV	L,A		
15C7	06	01		MOV B,L	1606	0D	1B	JTBL	DW		:INDIRECT JUMP TO PROC.
15C8	48			MOV C,B	1607	95	1A	DW	LET		:JMP TABLE
15C9	07			RLC	1608	8C	18	DW	END		:REM STMT. - NO ACTION
15CF	07			RLC	160C	13	10	DW	M1		:STOP STMT.-RETURN TO E
15D0	07			RLC	160E	F2	16	DW	GOTO		
15D1	07			RLC	1610	00	17	DW	IFRT		
15D2	E6	0F		ANI 17Q	1612	7D	1C	DW	INPUT		
15D3	E6	0F		ANI 17Q	1614	4C	18	DW	DIM		
15D4	E6	0F		ANI 17Q	1616	20	17	DW	CALLP		
15D5	CD	AD	12	CALL PAD	1618	0A	10	DW	GOSUB		
15D6	7A			MOV A,D	161C	E5	1D	DW	RETRN		
15D7	0D			MOV A,D	161E	7	1D	DW	FOR		
15D8	F2	D2	15	CALL FORM4	1620	D9	1E	DW	NEXT		
15D9	0D			CALL FORM4	16F2	2A	56	21	ENDD	LHLD KFPNT	:CHECK TO SEE IF MORE
15DA	0D			CALL FORM4	16F3	2A	A3	12	CALL	CHK1	:SOURCE AFTER END
15DB	0D			CALL FORM4	16F8	DA	13	10	JC	M1A	
15DC	0D			CALL FORM4	16F9	3E	05		MOV	A,3	:MORE SOURCE ERROR 3
15DD	0D			CALL FORM4	16FD	C3	BE	15	JMP	ERROR	
15DE	0D			CALL FORM4							
15DF	0D			CALL FORM4							
15E0	0D			CALL FORM4							
15E1	0D			CALL FORM4							
15E2	0D			CALL FORM4							
15E3	0D			CALL FORM4							
15E4	0D			CALL FORM4							
15E5	0D			CALL FORM4							
15E6	0D			CALL FORM4							
15E7	0D			CALL FORM4							
15E8	0D			CALL FORM4							
15E9	0D			CALL FORM4							
15EA	0D			CALL FORM4							
15EB	0D			CALL FORM4							
15EC	0D			CALL FORM4							
15ED	0D			CALL FORM4							
15EE	0D			CALL FORM4							
15EF	0D			CALL FORM4							
15F0	0D			CALL FORM4							
15F1	0D			CALL FORM4							
15F2	0D			CALL FORM4							
15F3	0D			CALL FORM4							
15F4	0D			CALL FORM4							
15F5	0D			CALL FORM4							
15F6	3E	07	16	THIS ROUTINE INCREMENTS H AND L AND DECR. C (CHARS IN LINE) SHOULD C RESULT IN 0 THEN THE ERROR CORRES. TO ENTRY PNT. IS GIVEN	1700	2A	5B	21	GOTC	LHLD CPNT	:GOTO STMT. PROC.
15F7	3E	08	16	ICP7: MVI A,7	1701	23		GSEAT	INX H	:INCREMENT 'PAST KEYWORD	
15F8	3E	08	16	ICP8: MVI A,8	1702	23			INX H		
15F9	3E	08	16	ICP9: MVI A,9	1703	23			INX H		
1600	3E	08	16	ICP10: MVI A,10	1704	23			INX H		
1601	3E	08	16	ICP11: MVI A,11	1705	23			INX H		
1602	3E	08	16	ICP12: MVI A,12	1706	23			INX H		
1603	3E	08	16	ICP13: MVI A,13	1707	23			INX H		
1604	3E	08	16	ICP14: MVI A,14	1708	23			INX H		
1605	3E	08	16	ICP15: MVI A,15	1709	23			INX H		
1606	3E	08	16	ICP16: MVI A,16	170A	23			INX H		
1607	3E	08	16	ICP17: MVI A,17	170B	23			INX H		
1608	3E	08	16	ICP18: MVI A,18	170C	23			INX H		
1609	3E	08	16	ICP19: MVI A,19	170D	23			INX H		
160A	3E	08	16	ICP20: MVI A,20	170E	23			INX H		
160B	3E	08	16	ICP21: MVI A,21	170F	23			INX H		
160C	3E	08	16	ICP22: MVI A,22	1710	23			INX H		
160D	3E	08	16	ICP23: MVI A,23	1711	23			INX H		
160E	3E	08	16	ICP24: MVI A,24	1712	23			INX H		
160F	3E	08	16	ICP25: MVI A,25	1713	23			INX H		
1610	3E	08	16	ICP26: MVI A,26	1714	23			INX H		
1611	3E	08	16	ICP27: MVI A,27	1715	23			INX H		
1612	3E	08	16	ICP28: MVI A,28	1716	23			INX H		
1613	3E	08	16	ICP29: MVI A,29	1717	23			INX H		
1614	3E	08	16	ICP30: MVI A,30	1718	23			INX H		
1615	3E	08	16	ICP31: MVI A,31	1719	23			INX H		
1616	3E	08	16	ICP32: MVI A,32	171A	23			INX H		
1617	3E	08	16	ICP33: MVI A,33	171B	23			INX H		
1618	3E	08	16	ICP34: MVI A,34	171C	23			INX H		
1619	3E	08	16	ICP35: MVI A,35	171D	23			INX H		
161A	3E	08	16	ICP36: MVI A,36	171E	23			INX H		
161B	3E	08	16	ICP37: MVI A,37	171F	23			INX H		
161C	3E	08	16	ICP38: MVI A,38	1720	23			INX H		
161D	3E	08	16	ICP39: MVI A,39	1721	23			INX H		
161E	3E	08	16	ICP40: MVI A,40	1722	23			INX H		
161F	3E	08	16	ICP41: MVI A,41	1723	23			INX H		
1620	3E	08	16	ICP42: MVI A,42	1724	23			INX H		
1621	3E	08	16	ICP43: MVI A,43	1725	23			INX H		
1622	3E	08	16	ICP44: MVI A,44	1726	23			INX H		
1623	3E	08	16	ICP45: MVI A,45	1727	23			INX H		
1624	3E	08	16	ICP46: MVI A,46	1728	23			INX H		
1625	3E	08	16	ICP47: MVI A,47	1729	23			INX H		
1626	3E	08	16	ICP48: MVI A,48	172A	23			INX H		
1627	3E	08	16	ICP49: MVI A,49	172B	23			INX H		
1628	3E	08	16	ICP50: MVI A,50	172C	23			INX H		
1629	3E	08	16	ICP51: MVI A,51	172D	23			INX H		
162A	3E	08	16	ICP52: MVI A,52	172E	23			INX H		
162B	3E	08	16	ICP53: MVI A,53	172F	23			INX H		
162C	3E	08	16	ICP54: MVI A,54	1730	23			INX H		
162D	3E	08	16	ICP55: MVI A,55	1731	23			INX H		
162E	3E	08	16	ICP56: MVI A,56	1732	23			INX H		
162F	3E	08	16	ICP57: MVI A,57	1733	23			INX H		
1630	3E	08	16	ICP58: MVI A,58	1734	23			INX H		
1631	3E	08	16	ICP59: MVI A,59	1735	23			INX H		
1632	3E	08	16	ICP60: MVI A,60	1736	23			INX H		
1633	3E	08	16	ICP61: MVI A,61	1737	23			INX H		
1634	3E	08	16	ICP62: MVI A,62	1738	23			INX H		
1635	3E	08	16	ICP63: MVI A,63	1739	23			INX H		
1636	3E	08	16	ICP64: MVI A,64	173A	23			INX H		
1637	3E	08	16	ICP65: MVI A,65	173B	23			INX H		
1638	3E	08	16	ICP66: MVI A,66	173C	23			INX H		
1639	3E	08	16	ICP67: MVI A,67	173D	23			INX H		
163A	3E	08	16	ICP68: MVI A,68	173E	23			INX H		
163B	3E	08	16	ICP69: MVI A,69	173F	23			INX H		
163C	3E	08	16	ICP70: MVI A,70	1740	23			INX H		
163D	3E	08	16	ICP71: MVI A,71	1741	23			INX H		
163E	3E	08	16	ICP72: MVI A,72	1742	23			INX H		
163F	3E	08	16	ICP73: MVI A,73	1743	23			INX H		
1640	3E	08	16	ICP74: MVI A,74	1744	23			INX H		
1641	3E	08	16	ICP75: MVI A,75	1745	23			INX H		
1642	3E	08	16	ICP76: MVI A,76	1746	23			INX H		
1643	3E	08	16	ICP77: MVI A,77	1747	23			INX H		
1644	3E	08	16	ICP78: MVI A,78	1748	23			INX H		
1645	3E	08	16	ICP79: MVI A,79	1749	23			INX H		
1646	3E	08	16	ICP80: MVI A,80	174A	23			INX H		
1647	3E	08	16	ICP81: MVI A,81	174B	23			INX H		
1648	3E	08	16	ICP82: MVI A,82	174C	23			INX H		
1649	3E	08	16	ICP83: MVI A,83	174D	23			INX H		
164A	3E	08	16	ICP84: MVI A,84	174E	23			INX H		
164B	3E	08	16	ICP85: MVI A,85	174F	23			INX H		
164C	3E	08	16	ICP86: MVI A,86	1750	23			INX H		
164D	3E	08	16	ICP87: MVI A,87	1751	23			INX H		
164E	3E	08	16	ICP88: MVI A,88	1752	23			INX H		
164F	3E	08	16	ICP89: MVI A,89	1753	23			INX H		
1650	3E	08	16	ICP90: MVI A,90	1754	23			INX H		
1651	3E	08	16	ICP91: MVI A,91	1755	23			INX H		
1652	3E	08	16	ICP92: MVI A,92	1756	23			INX H		
1653	3E	08	16	ICP93: MVI A,93	1757	23			INX H		
1654	3E	08	16	ICP94: MVI A,94	1758	23			INX H		
1655	3E	08	16	ICP95: MVI A,95	1759	23			INX H		
1656	3E	08	16	ICP96: MVI A,96	175A	23			INX H		
1657	3E	08	16	ICP97: MVI A,97	175B	23			INX H		
1658	3E	08	16	ICP98: MVI A,98							

MICROCOMPUTER DEVELOPMENT SOFTWARE

INTERFACE AGE 101

1A03	1A	LDAX	D	:AND PLACE ON STACK	1B3E	16 01	MVI	D,1	:SUPPRESS CR/LF
1A04	1F	MOV	D,A		1B40	CD 02 12	CALL	WRIT	
1A05	13	INX	D		1B43	C3 49 18	JMP	*+6	
1A06	13	LDAX	D		1B46	06 00 12	CALL	WRIT	:DUMP BUFFER, CONTINUE
1A07	13	INX	D		1B49	C3 8C 16	JMP	TEND	
1A08	67	MOV	H,A						
1A09	5F	XTHL		:XCHANGE, RESTORES H,L					
1A10	0A	CALL	AGA	:ANOTHER PASS?					
1A11	79	MOV	A,C	:GET 2ND VALUE	1B4C	79 5F 21	MOV	A,C	:IN CASE OF ERROR
1A12	07	ORA	A,C	:CHECK FOR END OF LINE	1B50	32 5B 21	LDAD	CPNT	:SAVE
1A13	27	1A		:IF SO => WELL FORMED	1B53	23	INX	H	:INPUT LINE (V-STRING)
1A14	C5	PUSH	B	:SAVE C	1B54	23	INX	H	:ADJUST PNTR'S
1A15	C5	PUSH	B	:ELSE CALL SYMSRT TO	1B56	CD F6 15	CALL	ICP7	
1A16	0D	CALL	SYMSRT	:CHECK FOR EXP. DEL.	1B59	CD F6 15	CALL	ICP7	
1A17	0D	CALL	SYMSRT	:RECOVER IT	1B5C	05	PUSH	H	:SAVE PNTR'S
1A18	0D	CALL	SYMSRT	:YES, WELL FORMED	1B5F	06 J1	PUSH	H	:SEND PROMPT
1A19	0D	CALL	SYMSRT	:ILL-FORMED EXP.	1B62	3E 3A	MOV	H,1	
1A20	0D	CALL	SYMSRT	:SAVE C, AND H,L	1B63	CD AD 12	CALL	PAD	:TO SUPPRESS CR/LF
1A21	0D	CALL	SYMSRT	:COPY 2ND VALUE TO	1B66	CD D2 12	CALL	WRIT	:PAU IT
1A22	0D	CALL	SYMSRT	:FREG2	1B69	21 01 21	LDX	H,1BUF	:ADD, JF INPUT BUFFER
1A23	0D	CALL	SYMSRT	:GET BYTES FROM STACK	1B6C	CD C9 13	CALL	TIYIN	:READ A LINE
1A24	0D	CALL	SYMSRT	:INTO FREG1+2	1B6F	05	PUSH	H	:ADD, OF K-STRING TO DE
1A25	0D	CALL	SYMSRT	:AND NEXT 2 BYTES	1B70	F1	PUSH	H	:ADD, OF V-STRING
1A26	0D	CALL	SYMSRT	:FROM STACK TO FREG1	1B71	F1	PUSH	H	:V-STRING CNT TO C
1A27	0D	CALL	SYMSRT	:GET OPERATION	1B72	02 9A 14	MOV	H,A	:V-STRING CNT TO B
1A28	0D	CALL	SYMSRT		1B73	CD 42 14	CALL	STRIN	:TRANSFER CONSTANTS TO
1A29	0D	CALL	SYMSRT		1B76	21 5A 14	J2	H,0DATA	:NO ERROR
1A30	0D	CALL	SYMSRT		1B77	CD 00 12	CALL	WRIT	:SEND ERROR MESSAGE
1A31	0D	CALL	SYMSRT		1B78	3A 5F 21	CALL	PLC	
1A32	0D	CALL	SYMSRT		1B79	05	PUSH	H	:GET V-STRING CNT
1A33	0D	CALL	SYMSRT		1B7C	CD 42 14	CALL	STRIN	:START AGAIN
1A34	0D	CALL	SYMSRT		1B7D	21 5A 14	J2	H,0DATA	:NEED MORE CONSTANTS
1A35	0D	CALL	SYMSRT		1B7E	CD 00 12	CALL	WRIT	:ALL OK - GET NEW PNTR.
1A36	0D	CALL	SYMSRT		1B7F	3A 5F 21	CALL	PLC	:CONT
1A37	0D	CALL	SYMSRT		1B80	05	PUSH	H	
1A38	0D	CALL	SYMSRT		1B81	05	PUSH	H	
1A39	0D	CALL	SYMSRT		1B82	05	PUSH	H	
1A40	0D	CALL	SYMSRT		1B83	05	PUSH	H	
1A41	0D	CALL	SYMSRT		1B84	05	PUSH	H	
1A42	0D	CALL	SYMSRT		1B85	05	PUSH	H	
1A43	0D	CALL	SYMSRT		1B86	05	PUSH	H	
1A44	0D	CALL	SYMSRT		1B87	05	PUSH	H	
1A45	0D	CALL	SYMSRT		1B88	05	PUSH	H	
1A46	0D	CALL	SYMSRT		1B89	05	PUSH	H	
1A47	0D	CALL	SYMSRT		1B8A	05	PUSH	H	
1A48	0D	CALL	SYMSRT		1B8B	05	PUSH	H	
1A49	0D	CALL	SYMSRT		1B8C	05	PUSH	H	
1A50	0D	CALL	SYMSRT		1B8D	05	PUSH	H	
1A51	0D	CALL	SYMSRT		1B8E	05	PUSH	H	
1A52	0D	CALL	SYMSRT		1B8F	05	PUSH	H	
1A53	0D	CALL	SYMSRT		1B90	05	PUSH	H	
1A54	0D	CALL	SYMSRT		1B91	05	PUSH	H	
1A55	0D	CALL	SYMSRT		1B92	05	PUSH	H	
1A56	0D	CALL	SYMSRT		1B93	05	PUSH	H	
1A57	0D	CALL	SYMSRT		1B94	05	PUSH	H	
1A58	0D	CALL	SYMSRT		1B95	05	PUSH	H	
1A59	0D	CALL	SYMSRT		1B96	05	PUSH	H	
1A60	0D	CALL	SYMSRT		1B97	05	PUSH	H	
1A61	0D	CALL	SYMSRT		1B98	05	PUSH	H	
1A62	0D	CALL	SYMSRT		1B99	05	PUSH	H	
1A63	0D	CALL	SYMSRT		1B9A	05	PUSH	H	
1A64	0D	CALL	SYMSRT		1B9B	05	PUSH	H	
1A65	0D	CALL	SYMSRT		1B9C	05	PUSH	H	
1A66	0D	CALL	SYMSRT		1B9D	05	PUSH	H	
1A67	0D	CALL	SYMSRT		1B9E	05	PUSH	H	
1A68	0D	CALL	SYMSRT		1B9F	05	PUSH	H	
1A69	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A70	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A71	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A72	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A73	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A74	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A75	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A76	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A77	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A78	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A79	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A80	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A81	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A82	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A83	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A84	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A85	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A86	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A87	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A88	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A89	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A90	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A91	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A92	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A93	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A94	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A95	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A96	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A97	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A98	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A99	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A00	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A01	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A02	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A03	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A04	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A05	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A06	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A07	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A08	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A09	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A10	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A11	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A12	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A13	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A14	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A15	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A16	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A17	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A18	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A19	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A20	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A21	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A22	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A23	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A24	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A25	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A26	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A27	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A28	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A29	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A30	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A31	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A32	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A33	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A34	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A35	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A36	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A37	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A38	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A39	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A40	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A41	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A42	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A43	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A44	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A45	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A46	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A47	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A48	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A49	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A50	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A51	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A52	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A53	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A54	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A55	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A56	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A57	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A58	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A59	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A60	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A61	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A62	0D	CALL	SYMSRT		1BA3	05	PUSH	H	
1A63	0D	CALL	SYMSRT		1BA4	05	PUSH	H	
1A64	0D	CALL	SYMSRT		1BA5	05	PUSH	H	
1A65	0D	CALL	SYMSRT		1BA6	05	PUSH	H	
1A66	0D	CALL	SYMSRT		1BA7	05	PUSH	H	
1A67	0D	CALL	SYMSRT		1BA8	05	PUSH	H	
1A68	0D	CALL	SYMSRT		1BA9	05	PUSH	H	
1A69	0D	CALL	SYMSRT		1BA0	05	PUSH	H	
1A70	0D	CALL	SYMSRT		1BA1	05	PUSH	H	
1A71	0D	CALL	SYMSRT		1BA2	05	PUSH	H	
1A72	0D	CALL	SYMSRT		1BA3				

MICROCOMPUTER DEVELOPMENT SOFTWARE

INTERFACE AGE 103


```

1ED0 FF 96 CPI TOPNS AND 3770 ;NEED ONLY COMPARE PAGE
1ED1 CA 0B 1F NSTOK: JZ FRI8 ;FUR'S NEXTED TWO DEEP
1ED2 CD 2A 2C 21 ;SAVE NEST SP ;SAVE NEST SP
1ED3 CD 2A 2C 21 ;SAVE IT ;UPDATE NEST SP
1ED4 CD 2A 2C 21 ;SAVE IT ;SAVE IT
1ED5 CD 2A 2C 21 ;RESTORE OLD SP ;RESTORE OLD SP
1ED6 CD 2A 2C 21 ;ALL DONE ;FLOATING PNT ONE
1ED7 CD 2A 2C 21 ;NEXT STATEMENT PROC SSOR
1ED8 CD 2A 2C 21 ;NEXT: LHLH CPNT ;FIX PNTR'S
1ED9 CD 2A 2C 21 ;INX H ;INX H
1EDA CD 2A 2C 21 ;INX H ;INX H
1EDB CD 2A 2C 21 ;INX H ;INX H
1EDC CD 2A 2C 21 ;CALL LCP7 ;LETTER?
1EDD CD 2A 2C 21 ;CALL ALPHA ;LETTER?
1EDE CD 2A 2C 21 ;JNC FR21 ;NO, ERKOR
1EDF CD 2A 2C 21 ;MOV M ;NO, GET IT
1EE0 CD 2A 2C 21 ;MOV M ;SAVE C
1EE1 CD 2A 2C 21 ;MOV M ;INIT C TO 0
1EE2 CD 2A 2C 21 ;MOV M ;BUMP PNTR'S
1EE3 CD 2A 2C 21 ;CALL NEXT1 ;NEXT1
1EE4 CD 2A 2C 21 ;CALL NUMB ;NUMBER?
1EE5 CD 2A 2C 21 ;JNC ER21 ;NO, ERROR
1EE6 CD 2A 2C 21 ;JNC ER21 ;YES, GET IT
1EE7 CD 2A 2C 21 ;JNC ER21 ;C-M
1EE8 CD 2A 2C 21 ;JNC ER21 ;D
1EE9 CD 2A 2C 21 ;JNC ER21 ;D
1EEA CD 2A 2C 21 ;JNC ER21 ;D
1EEB CD 2A 2C 21 ;JNC ER21 ;D
1EEC CD 2A 2C 21 ;JNC ER21 ;D
1EED CD 2A 2C 21 ;JNC ER21 ;D
1EEF CD 2A 2C 21 ;JNC ER21 ;D
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1FFE CD 2A 2C 21 ;JNC ER21 ;D
1FFF CD 2A 2C 21 ;JNC ER21 ;D

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NO PROGRAM ERRORS

SYMBOL TABLE

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* 01 0307 ADDJ 1A56 ADFLD 1812 AFUND 190F
AGA 1A02 ALPHA 1222 AR 1614 AREK 1889
ARVES 18CD ASHC 1A59 B 0300 BAC 1220
BINOP 1A10 BOUTR 1988 BND1 150C BND2 1889
BND3 15A6 BOUTN 21AA BOUND 154D BOUT 1890
CHAR5 0301 C1 1219 CALLP 105A CHAR2 0FF7
CLSUB 10CC CUNT 1778 CONV 0F55 CHMO 1887
COPDH 17AB CPNT 1758 LK REG 12A0 CUPD1 17AE
CVB1 124B CVM2 126B DIV 0002 CVP 122A
DFXL 0FDC DIM 1720 DIV 1A80 DLOPP 0FF1
DUL 19EC EOK 19FA DIV 1A80 ENDD 16F3
ENTRY 1671 EOK 19FA DIV 1A80 ENDD 16F3
ER16 1F81 FR17 1F86 ER10 1C78 ER19 1F90
ER20 1095 FR17 1F86 ER10 1C78 ER19 1F90
ER8 1A22 ER9 1F7C ERLN 150F ERRET 18C8
ERKOR 125E ERLN 150F EVAL 19C7 EXPRE 1A06
F1 144E FALSE 1012 FBAC 1576 FBIL 1668
FCUMP 1023 FDATE 196F FFXT 1E80 FINPT 0F8F
FIX 1915 FONE 1E29 FLINT 2190 FMUL 1A67
FND5B 108E FONE 1E29 FINT 10E7 FORM2 1447
FOR11 1440 FOR12 143F FORM1 1448 FORM3 1447
FOR13 1444 FOR14 1447 FORM2 1447 FORM4 1447
FOR17 1444 FORM8 1443 FORM3 1447 FORM5 1447
PPERAR 1A5B FREG1 217C FREG2 2180 FSYM 160D
PAM 21AA GOT1 1700 GREG 2177 GSENT 1703
GOSUB 10D0 H 0004 HLINP 2181 HUME 1824
GIRA 1709 H 1C80 ILIN 2181 LNC 1885
HSTRIN 1405 H 1C80 ILIN 2181 LNC 1885
ICP4 1630 ICP7 1F5F ICP8 15F8 IDONE 1963
IEND 188C INP 1973 INPR 1CAB INPK 168C
INCP1 1607 INP 1973 INPR 1CAB INPK 168C
INPUT 194C INP 1973 INPR 1CAB INPK 168C
ISR12 117A ISRT1 1007 ISRT5 110F ISRT6 1121
ISR17 1146 ISRT8 1148 ISRT9 1152 ISRT10 1171
KASE 1260 KDATA 134B KDATA 134B KDATA 134B
KDATA 134B KDATA 134B KDATA 134B KDATA 134B
KL4 155A KL6 215B KL6 215B KL6 215B KL6 215B
KONT 183B KONT 183B KONT 183B KONT 183B
LADD 0FDD LDIV 0FDD LDIV 0FDD LDIV 0FDD
LET 180D LOK 18ED LOK 18ED LOK 18ED LOK 18ED
LMUL 0FDD LOK 18ED LOK 18ED LOK 18ED LOK 18ED
LUKDN 1627 LOK 18ED LOK 18ED LOK 18ED LOK 18ED
M2 0916 M2 0916 M2 0916 M2 0916 M2 0916
MCHK 0FF4 MCHK 0FF4 MCHK 0FF4 MCHK 0FF4 MCHK 0FF4
MEMST 2100 MEMST 2100 MEMST 2100 MEMST 2100 MEMST 2100
MODE1 1997 MODE1 1997 MODE1 1997 MODE1 1997 MODE1 1997
MUL12 2164 MUL12 2164 MUL12 2164 MUL12 2164 MUL12 2164
NEXT1 1E10 NEXT1 1E10 NEXT1 1E10 NEXT1 1E10 NEXT1 1E10
NL6 2151 NL6 2151 NL6 2151 NL6 2151 NL6 2151
NOENT 1646 NOENT 1646 NOENT 1646 NOENT 1646 NOENT 1646
NOT3 1008 NOT3 1008 NOT3 1008 NOT3 1008 NOT3 1008
NUSUB 107D NOT3 1008 NOT3 1008 NOT3 1008 NOT3 1008
ODAD 1468 ODATA 1468 ODATA 1468 ODATA 1468 ODATA 1468
ODAT4 1481 ODATA 1468 ODATA 1468 ODATA 1468 ODATA 1468
ODAT8 1487 ODATA 1468 ODATA 1468 ODATA 1468 ODATA 1468
OKLET 1731 OKN 1731 OKN 1731 OKN 1731 OKN 1731

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P1 12B8 P2 12C2 PAD 12AD PARL 1D9D
PEND 1846 PINL 140B PK2 140E PIN3 150D
PINT 1C73 PK1 1418 PL2 215B
PL4 215D PK1 1418 PL2 215B
PREXP 10B5 PRI 1A95 PR1 1A95
PTFIN 1C4C PTVAL 0FEE PT1 106D
QSTR1 1430 QSTRG 142B QSTRG 142B
QUOTE 1A84 QSTRG 142B QSTRG 142B
RINST 1834 RUN 1678 S2 1307
S4 1323 S4 1322 S4 1322
SBSAV 2150 S4 1322 S4 1322
SCULN 1807 SCR 2166 SCALR 1881
SINEQ 1038 SLOAD 18AA SEND 0006
SP 0006 SPACE 1981 SONMO 1839
STNER 18C8 STRIN 1892 STAL 2196
STPNT 1188 SUBB 1A81 SUBS 21AC SYMSR 1277
THEN 1019 TINI 13CC TIN2 13F9
TIN4A 140B TIN5 1401 TIN5A 1404
TRUE 1016 TTYIN 13C9 V1 1815
VAR 186D VARAD 218A VEND 21A1
VNAME 1876 VNAME 1876 VNAME 1876
WPPER 1876 WPPER 1876 WPPER 1876
ZROL OFCO ZROL OFCO ZROL OFCO

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JABBERWOCKY.

'Twas brillig, and the slithy toves
 Did gyre and gimble in the wabe;
 All mimsy were the borogoves,
 And the mome raths outgrabe.

"Beware the Jabberwock, my son!
 The jaws that BYTE, the claws that catch!
 Beware the Jubjub bird, and shun
 The frumious Bandersnatch!"

He took his vorpal sword in hand:
 Long time the manxome foe he sought—
 So rested he by the Tumtum tree,
 And stood awhile in thought.

And as in uffish thought he stood,
 The Jabberwock, with eyes of flame,
 Came whiffing through the tulgey wood,
 And burbled as it came!

One, two! One, two! And through and through
 The vorpal blade went snicker-snack!
 He left it dead, and with its head
 He went galumphing back.

"And hast thou slain the Jabberwock?
 Come to my arms, my beamish boy!
 O frabjous day! Callooh! Callay!"
 He chortled in his joy.

'Twas brillig, and the slithy toves
 Did gyre and gimble in the wabe;
 All mimsy were the borogoves,
 And the mome raths outgrabe.

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By Mark Alexander

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Santa Clara, CA

INTRODUCTION

NIBL (National Industrial Basic Language) is a conversational programming language for the SC/MP. It is a language similar to Tiny BASIC Extended, but it also has some unique features. Many of these features, such as a genuinely useful control structure (the PASCAL-influenced DO/UNTIL) and the indirect operator ("@") have been added to the language to allow NIBL to be nearly as flexible as machine language in such applications as medium-speed process control.

By using NIBL, one trades the high execution speed and low memory consumption of machine language for some very tangible advantages: program readability and modifiability which are truly difficult to achieve in machine language programs.

NIBL programs are interpreted by a large (4K byte) TBX SC/MP program that resides in ROM. The interpreter is broken into two main blocks: a program written in an Intermediate (or Interpretive) Language — IL for short — which does the actual interpretation; and a collection of SC/MP machine language subroutines invoked by the IL program. The IL approach is well-documented in vol. 1, no. 1 of *Dr. Dobbs' Journal of Computer Calisthenics and Orthodontia*, and readers should refer to that issue for a more detailed description of the interpretation process.

In Table 1, the formal grammar for NIBL is given. This is the ultimate authority (other than the interpreter itself) on how legal NIBL statements are formed. The following descriptions of the NIBL statements will refer to portions of the grammar. Table 2 contains a list of the error messages produced by the NIBL system. Finally, a listing of the NIBL interpreter is given.

Table 1: NIBL grammar

On reading the grammar:

All items in single quotes are actual symbols in NIBL; all other identifiers are symbols in the grammar. The equals sign "=", means "is defined as"; parentheses are used to group several items together as one item; the exclamation point, "!", means an exclusive or choice between the items on either side of it; the asterisk, "*", means zero or more occurrences of the item to its left; the plus sign, "+", means one or repetitions; the question mark, "?", means zero or one occurrences; and the semicolon, ";", marks the end of a definition.

NIBL Line	= Immediate Statement ! Program Line ;
Immediate Statement	= (Command ! Statement) Carriage Return;
Program Line	= (Decimal Number Statement List Carriage Return);
Command	= 'NEW' ! 'CLEAR' ! 'LIST' Decimal Number ? ! 'RUN' ;
Statement List	= Statement (':' STATEMENT) *;
Statement	= 'LET' ? Left part '=' Rel Exp ! 'LET' ? '\$' Factor '=' (String ! '\$' Factor) ! 'GO' ('TO' ! 'SUB') Rel Exp ! 'RETURN' ! ('PR' ! 'PRINT') Print List ! 'IF' Rel-Expr 'THEN' ? Statement ! 'DO' ! 'UNTIL' Rel-Exp ! 'FOR' Variable '=' Rel Exp 'TO' Rel Exp ('STEP' Rel Exp) ? ! 'NEXT' Variable ! 'INPUT' (Variable + ! '\$' Factor) ! 'LINK' Rel Exp ! 'REM' Any Character Except Carriage Return + ! 'END' ;
Left Part	= (Variable ! '@' Factor ! 'STAT' ! 'PAGE') ;
Rel Exp	= Expression Relop Expression ! Expression ;
Relop	= '<' ! '<' '=' ! '<' '>' ! '>' ! '>' '=' ! '=' ;
Expression	= Expression Adding Operator term ! ('+' ! '-') ? Term ;
Adding Operator	= '+' ! '-' ! 'OR' ;
Term	= Term Multiplying Operator Factor ! Factor ;
Multiplying Operator	= '*' ! '/' ! 'AND' ;
Factor	= Variable ! Decimal Number ! '(' Rel Exp ')' ! '@' Factor ! '#' Hex Number ! 'NOT' Factor


```

! 'MOD' '(' Rel Exp ',' Rel Exp ')'
! 'RND' '(' Rel Exp ',' Rel Exp ')'
! 'STAT'
! 'TOP'
! 'PAGE'
;

```

Variable = 'A' | 'B' | 'C' | ... | 'Y' | 'Z' ;

Decimal Number = Decimal Digit + ;

Decimal Digit = '0' | '1' | '2' | ... | '9' ;

Hex-Number = (Decimal Digit | Hex Digit) + ;

Hex Digit = 'A' | 'B' | 'C' | 'D' | 'E' | 'F' ;

Print List = Print Item + ;

Print Item = (String | Rel Exp | '\$' Factor) ;

String = '' Almost Any Character '' ;

NOTE: Spaces are not usually significant in NIBL programs, with the following exceptions: spaces cannot appear within key words (such as 'THEN' or 'UNTIL') or within constants. Also, a variable (such as A or Z) must be followed immediately by a non-alphabetic character to distinguish it from a key word.

Table 2: NIBL error messages

Error messages are of the form:

EEEE ERROR AT LN

where EEEE is one of the error codes below, and LN is the number of the line in which the error was encountered.

AREA	No more room left for program in current page
CHAR	Character after logical end of statement
DIV0	Division by zero
END"	No ending quote on string
FOR	FOR without NEXT
NEST	Nesting limit exceeded in expression, FOR's, GOSUBs, etc.
NEXT	NEXT without FOR
NOGO	No line number corresponding to GOTO or GOSUB
RTRN	RETURN without previous GOSUB
SNTX	Syntax error
STMT	Statement type used improperly
UNTL	UNTIL without DO
VALU	Constant format or value error

HISTORY OF NIBL

NIBL came into this world as an interpreter for Tiny BASIC, as originally described in the first issue of Dr. Dobb's Journal. That program was written by Steve Leininger, who subsequently left before the program was ever assembled or executed. The current version of NIBL is an almost complete re-write of the original interpreter, with changes and additions being made to improve the modularity of the program, to greatly increase execution speed, and to extend the capabilities of the language itself.

SYSTEM REQUIREMENTS

The NIBL interpreter is intended to be a ROM-resident program in the first 4K of the SC/MP Memory address space (although it will run just as well in RAM). The interpreter requires at least 2K bytes of RAM starting at address 1000 (base 16), of which the interpreter uses nearly 300 bytes for stacks, variables,

etc., leaving the rest for the user's program. Another 2K bytes of memory may be added to fill up this 4K page, forming what is hereafter referred to as "Page 1."

The SC/MP architecture forces memory to be split into pages of 4K bytes each; therefore, NIBL allows seven such pages to be used for storing programs. NIBL programs in the seven pages are edited separately, but may be linked together during program execution by special NIBL statements described in the following pages. Page #1 as mentioned above, must be RAM since the interpreter uses part of it as temporary storage; the part used to store application programs starts at location 111E (base 16).

The other six pages of memory, each of which starts at location n000 (base 16), where n is the page number, may be either RAM or ROM. Page 2 is a special page: it can contain a NIBL program to be executed immediately upon powering up the NIBL system.

The memory organization of NIBL is shown in Figure 1.

Throughout this article, the assumption is made that the user has a teletype with paper tape reader and punch, as with the SC/MP Low Cost Development System (LCDS). In fact, NIBL was designed to use the SC/MP LCDS teletype interface, but to be completely independent of the LCDS firmware. If NIBL is to be run on its own, the system should have the same configuration for the teletype, with the reader relay being operated directly by the SC/MP. At present, paper tape is the only medium for saving NIBL programs, but as soon as the hardware and software for a SC/MP cassette interface become available, NIBL will be able to link to routines for saving and loading programs with ease.

Since the teletype interface is not based on a UART, the terminal baud rate can only be changed by modifying the timed delays in NIBL's I/O routines. NIBL has been run successfully at 1200 baud with a CRT terminal; the assembly listing of the NIBL program is programmed for a 110 baud rate system.

COMMUNICATING WITH NIBL

When the NIBL system is ready to accept input, it prompts at the teletype with a ">" prompt sign. (NIBL is now in "edit mode.") The user then enters a line terminated by a carriage return. There are several special characters that are used to edit lines as they are typed:

Shift/O (back-arrow) causes the last character typed to be deleted.

Control/H (backspace) performs the same function as shift/O, but echoes as a backspace/space/backspace sequence, which is only useful if the teletype routines are modified to run at high baud rates for use with CRT's.

Control/U (echoed as " U") causes the entire line to be deleted; NIBL reprompts for a new line.

Entering a line to NIBL without a leading line number causes the line to be executed directly by NIBL. Most NIBL statements, as well as the four program control commands, may be executed in this manner.

A line with a leading number (in the range 0 through 32767) is entered into the NIBL program in the cur-

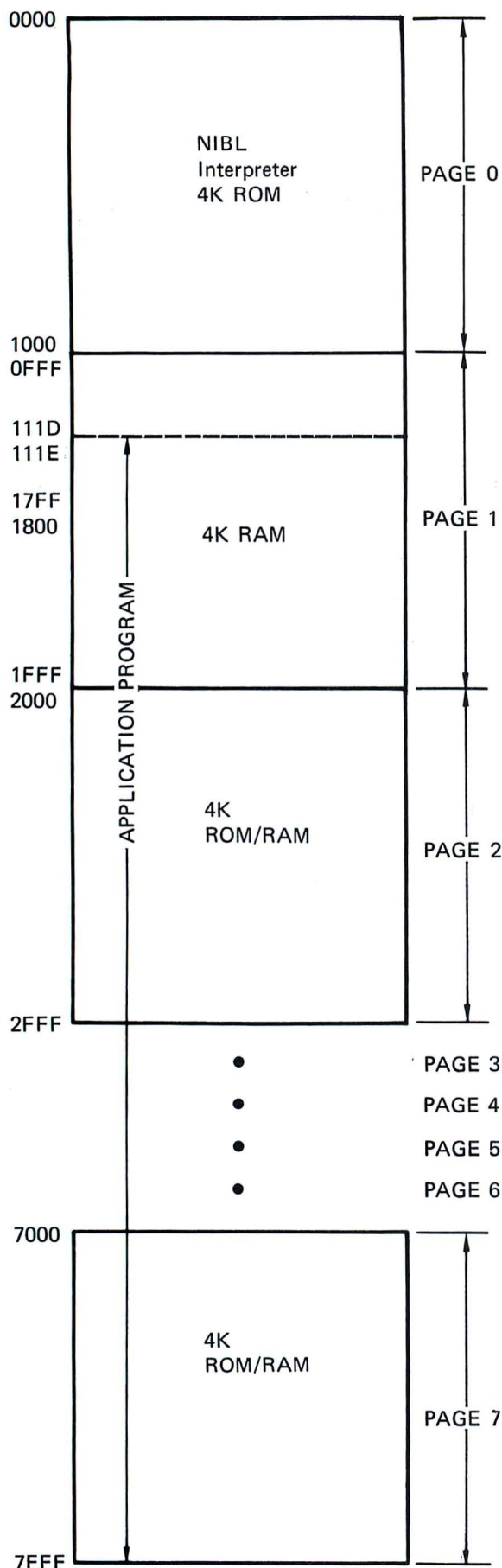


FIGURE 1. NIBL MEMORY ORGANIZATION

rent page. (Make sure that the value of the pseudo-variable PAGE is valid, so that the line isn't lost into non-existent memory.) The NIBL editor sorts the program lines as they are entered into ascending order by line number.

Typing a line number followed by a carriage return deletes that line from the program. Typing a line with the same number as an existing line's causes the new line to replace the old one in the program.

Each of the seven memory pages may contain a different program, separate from the rest. Editing the program in one page will not affect the other pages. To switch editing from one page to another, simply type PAGE = n, where n is the number of the new page.

VARIABLES

There are twenty-six variable names in NIBL: the letters A through Z. They are all 16-bit binary variables, so they can be used to hold addresses as well as signed numeric data. Space for pre-declared variables is allocated for them in RAM when NIBL powers up.

CONSTANTS

NIBL allows either decimal or hexadecimal (base 16) constants to appear in expressions. Decimal constants must lie in the range 0 through 32767; the unary minus ("−") is used to obtain negative values. The value −32768 is a valid NIBL integer, but it is not legal as it stands. To represent it, use −32767-1 or #8000 instead.

Hexadecimal constants are denoted by a pound sign ("#") followed by a string of hexadecimal digits (0-9, A-F). NIBL does not check for overrun in hex constants; consequently, only the 4 least significant digits of the hex digit string are kept.

FUNCTIONS

NIBL includes three functions that may appear in any expression. These are described as follows:

RND (X, Y) returns a pseudo-random integer in the range X through Y, inclusive, where X and Y are arbitrary expressions. In order for the function to work properly, the value of Y − X should be positive and no greater than 32767.

MOD (X, Y) returns the absolute value of the remainder from X divided by Y (where X and Y are expressions).

TOP (with no arguments) returns the address of the first free byte in the memory page currently being edited or executed. In other words, it is the address of the last byte at the top of the current NIBL application program in the current page, plus one.

PSEUDO-VARIABLES

NIBL has two pseudo-variables in addition to the standard variables. These are STAT and PAGE. Both of these variables may appear on either side of an assignment statement.

STAT represents the SC/MP status register. The current value of the status register can be referred to by using STAT in an expression; or an assignment may

be made to the status register by executing a statement such as `STAT = 4` or `STAT = STAT OR #20`. When NIBL makes an assignment to the status register in this manner, it clears the interrupt-enable bit of the value before it is actually assigned. Note also that only the lower byte of the value is assigned, the high byte is ignored.

The carry and overflow bits in STAT are meaningless since the NIBL system is continually modifying them. The utility of STAT lies in the fact that 5 of its bits are connected to I/O sense lines on the SC/MP chip.

The pseudo-variable PAGE contains the number of the memory page currently being executed or edited. As indicated in Figure 1, there are seven pages in which NIBL programs may be stored; therefore, the PAGE number may be only in the range of 1 through 7. If an assignment of a value outside this range is made to PAGE, only the 3 least significant bits (LSBs) of the value are used. Page one is defined as `LSBs = 000`, page two as `LSBs = 001` etc.

If PAGE is modified while NIBL is in edit mode, all subsequent editing will take place in the new page.

If PAGE is modified by a NIBL program during execution, control will be passed to the first line of the NIBL program in the new page. This transfer would be effected by a statement such as `PAGE = 6` or `PAGE = PAGE + 1`. Thus, several NIBL programs residing in different 4K pages may be linked together as one large program, if need be. This would allow one to write a 28K STAR TREK program in NIBL, a Herculean and indeed foolish task.

Control may also be transferred from one page to another by three other statements: RETURN, NEXT, and UNTIL. Thus, the first part of a subroutine or loop may be in one page, and the second part may be in another (with control being transferred between the two parts by an assignment to PAGE). In these three special cases, NIBL automatically updates the value of PAGE as the statements are executed.

RELATIONAL OPERATORS

NIBL provides the standard BASIC relational operators, for comparing the values of integer expressions. The operators are as follows:

- = equal to
- <= less than or equal to
- >= greater than or equal to
- <> not equal to
- < less than
- > greater than

All of these operators produce 1 as a result if the relation is true, and 0 if the relation is false. Note that the relational operators may appear anywhere that an expression is called for in the NIBL grammar, not only in IF statements.

ARITHMETIC OPERATORS

NIBL provides the four standard arithmetic functions: addition (+), subtraction or unary minus (-), multiplication (*), and division (/). Since only integers are allowed in NIBL, all quotients are truncated (the

MOD function can be used to obtain remainders from division). Any overflow or underflow (other than division by zero) is ignored by NIBL; the reasoning behind this is that it may often be necessary to treat NIBL expressions as unsigned values, such as when performing calculations using memory addresses as the operands. Thus the value of `32767 + 1` is `-32768` (or in hexadecimal, `°7FFF + 1 = #8000`, which makes more sense).

LOGICAL OPERATORS

In NIBL, there are three logical operations that may be performed on values: AND, OR, and NOT. The first two are binary operators, and the latter is unary. All three perform bitwise logical operations on 16-bit arguments, producing 16-bit results. AND, OR, and NOT are sufficient to simulate any other logical operation, through various combinations of the operators.

THE INDIRECT OPERATOR

The indirect operator "@" realizes the functions of PEEK and POKE operations in other BASICs, but with somewhat more elegance. The "@" sign followed by an address (which can be a constant, variable, or expression in parentheses) denotes the contents of that address in memory. Thus, if memory location 245 (decimal) contains 60, the statement `X=@245` would result in the value 60 being assigned to X. The indirect operator may also appear on the left side of an assignment statement. For example, `@X=@(Y+10)` would result in the memory location pointed to by X being assigned the value of the memory location pointed to by the value Y+10.

Use of the indirect operator is not limited to reading from or writing to memory: it also provides a simple way to communicate with peripheral devices that are interfaced to the SC/MP through memory addresses. Note that the "@" operator can only access memory one byte at a time, and that when an assignment is made to a memory location, only the low order byte of the value is moved to the location; the high order byte is ignored.

The indirect operator can also be used to simulate arrays in NIBL. For example, if we wish to define an M x N matrix of one-byte positive integers, we can access the (I,J)th element of the matrix (assuming that (0,0) is a legal element in the matrix) with the expression `@(A+I*N+J)`. An assignment could be made to that same element by placing the expression on the left side of an assignment statement.

EXPRESSIONS

Expressions in NIBL are composed of variables, constants, function references, pseudo-variables, and operators. Operators bind these other elements together to form complete expressions. NIBL expressions are all 16-bit integers. Evaluation of expressions takes place left-to-right, and the order in which operations take place is determined by operator precedence and the presence of parentheses. The order of evaluation can be deduced from the grammar in Table 1; here is a table of operator precedence:

Lowest precedence (applied last): $<$, $>$, $<=$, $>=$, $=$,
 $<>$
 $+$, $-$, OR
 $*$, $/$, AND

Highest precedence (applied first): $@$, NOT

Despite this, it is still safest to use plenty of parentheses in expressions to make the intent clear.

PROGRAM CONTROL COMMANDS

LIST causes the entire program in the current page to be listed. Listing can be halted by hitting any key on the teletype: the BREAK key works best.

LIST $<\text{number}>$ causes listing to begin at the given line number (or the nearest one greater than the number), rather than at the first line.

LISTing a program is the method used to save it on paper tape. To accomplish this, type LIST with the punch off, then turn on the punch and hit carriage return. After the program is dumped, type a Shift/O with teletype on LOCAL so that the last character (a $">"$) will be deleted when the tape is entered to NIBL at a later time. NIBL will accept a tape made in this fashion at any time during edit mode. The tape reader is enabled at all times by NIBL, and it does not distinguish between the reader and the keyboard when accepting input. Superfluous line-feed and null characters on the tape are echoed but ignored.

RUN causes three actions: first, all variables are zeroed; secondly, all stacks (the FOR, DO, and GOSUB stacks) are cleared; and finally the program in the current page is executed, starting with the first line in sequence.

RUN is not the only way to start program execution: GOTO and GOSUB can also be used to jump into a program from edit mode. For example, if there is a subroutine at line 1000 that is being tested, typing GOSUB 1000 will cause that routine to be executed, with NIBL returning to edit mode upon encountering a RETURN statement. When GOTO and GOSUB are used to run a program, the variables and stacks are not cleared.

Hitting any key while a program is being run will cause NIBL to break execution, printing a message and the line number where the break was detected. The BREAK key on the teletype works best for this.

CLEAR causes all variables to be zeroed and the three stacks mentioned above to be cleared. This latter feature of the CLEAR command is quite useful after a stack nesting error has occurred (for example, if GOSUBs are nested more than eight levels deep).

NEW clears the program in Page 1, and changes the value of PAGE to 1. This is the form of the command most likely to be used by NIBL novices who do not wish to be confused by the page selection features of NIBL. NEW should be the first thing one types in to NIBL when first powering up.

NEW $<\text{number}>$ sets the value of PAGE to the $<\text{number}>$, and clears the program in that page.

ASSIGNMENT STATEMENTS

Previously, two different types of assignment state-

ments have been described: assignments to the pseudo-variables STAT and PAGE, and assignments to memory locations with the indirect operator. Another form of the assignment statement is the conventional assignment to a variable ($A = Z$), e.g. $A = A + 1$ or $A = 32 < (4 * I)$. There are also statements which look like string assignments, but these are not standard BASIC, and are described later in the section on string handling. The word "LET" is optional in front of any assignment statement (leaving it out increases execution speed, unlike most Tiny BASIC systems).

IF/THEN STATEMENT

The IF statement allows conditional execution of one or more statements (as many as can fit on one line). The syntax for the IF statement is:

'IF' Rel-exp 'THEN'? Statement

which indicates that the word THEN is optional, and that any statement (including another IF statement) may follow the conditional expression. If the IF condition is true (i.e. is non-zero), the statement following it (and any others on the line) will be executed; otherwise, control immediately transfers to the next program line. The condition does not need to contain relational operators: a statement such as IF MOD (A, 5) THEN ... is perfectly legal. In this example, the statement following the THEN would be executed if A were not divisible by 5.

GOTO, GOSUB, AND RETURN STATEMENTS

The syntax for the GOTO statement is 'GOTO' followed by an expression. The effect of the GOTO statement is to transfer control to the line whose number is indicated by the expression. An error occurs if the specified line does not exist in the current page. Unlike standard BASICs, any arbitrary expression can be used to specify the line number, as well as the usual decimal constant. This allows computed branches to be performed with the same effect as the ON ... GOTO statement in standard BASIC.

The GOSUB statement is identical to the GOTO statement in form. It too causes a branch to a new line, but it also saves the address of the following statement on a stack. When a RETURN statement is executed, the saved address is popped from the stack, and control returns to that point in the program. Since an actual address, not a line number, is saved on the GOSUB stack, GOSUB statements may appear anywhere on a multiple-statement line.

GOSUBs may be nested up to eight levels deep; an error will occur if an attempt is made to exceed this limit. The error condition does not destroy the previous contents of the stack, so a RETURN statement can be executed (even in edit mode) without an error occurring. However, any modification of the NIBL program will clear the GOSUB stack, so that a subsequent RETURN without a GOSUB will cause an error.

DO AND UNTIL STATEMENTS

The DO and UNTIL statements are useful in writing program loops efficiently, without using misleading

GOTO statements. Enclosing a group of zero or more statements between a DO statement and an UNTIL <condition> statement (where <condition> is an arbitrary expression) will cause the statement group to be repeated one or more times until the <condition> becomes true (i.e. non-zero). As an example of the use of the DO and UNTIL statements, we present a program that prints the prime numbers:

```
10 PRINT 1: PRINT 2
20 I=3
30 DO
40 J=I/2: N=2
50 DO
60 N=N+2
70 UNTIL (MOD (I, N) = 0) OR (N>J)
80 IF N>J PRINT I
90 I=I+2
100 UNTIL 0
```

DO loops may be nested up to eight levels deep, and NIBL acts in the same manner if an overflow occurs as it does with a GOSUB overflow. NIBL also reports an error if an UNTIL statement occurs without a previous DO. A single DO loop may have more than one UNTIL statement as a terminator. For example, if one wished to exit abnormally out of a DO loop and transfer to some appropriate line, it could be done in the following manner:

```
UNTIL 1: GOTO X
```

where X is the line number.

Neither the DO nor the UNTIL statement may be executed in edit mode.

FOR AND NEXT STATEMENTS

The NIBL FOR statement is virtually identical to that in standard BASICs; consequently, it is not explained in great detail here.

As in most BASICs, both positive and negative STEPs are allowed in the FOR statement, and a STEP of +1 is assumed if the STEP portion of the statement is omitted. A FOR loop is terminated by a NEXT <variable> statement, and the <variable> must be the same as that referred to in the FOR statement at the beginning of the loop.

FOR loops may be nested four levels deep; NIBL reports an error if this limit is exceeded, or if a NEXT statement occurs without a previous FOR statement. As with the DO and UNTIL statements, FOR and NEXT may not be executed in edit mode.

Perhaps the only differences between the NIBL FOR statement and that of more elaborate BASICs (such as DEC's BASIC-PLUS for the PDP-11) are that a FOR loop is always executed at least once, and that when a NEXT statement is executed, the STEP value is added to the variable before the test is made to determine if the loop should be repeated (rather than after the test).

INPUT STATEMENT

There are two types of INPUT statements in NIBL: numeric input and string input. The form of the first type is 'INPUT' followed by a list of one or more variables. When this statement is executed, NIBL prompts

at the teletype with a question mark ("?"). The user responds with a list of expressions separated by commas, and terminated by a carriage return. For example, a legal response to the statement INPUT A,B,C would be #3FA,26,4*27. These three expressions would then be assigned to the variables A,B, and C, respectively. An illegal response (too few arguments or improper expressions) will result in a syntax error. Any extra arguments in the response are ignored.

The second type of INPUT statement allows strings to be input. The form of the statement is 'INPUT' '\$' <address>, where <address> is a Factor, syntactically (usually a variable, constant, or expression in parentheses). When this statement is executed, NIBL prompts the user as before, at which point the user enters a line terminated by the usual carriage return. NIBL then stores the line in memory in consecutive locations, beginning at the address specified. Thus, INPUTS #6000 would cause the input line to be stored starting at location 6000 (base 16); the carriage return would also be stored at the end of the line.

Strings input in this manner can be tested and manipulated by using the "@" operator or the string handling statements described below. They can also be displayed by a PRINT statement.

Neither of the two INPUT statements may be executed in edit mode.

PRINT STATEMENT

The form of the PRINT statement is 'PRINT' or 'PR' followed by a list of print items separated by commas, and optionally terminated by a semicolon, which suppresses an otherwise automatic carriage return after all items in the list are printed.

A print item consists of one of the following:

- A quoted string, which is printed exactly as it appears (with the quotes removed)
- An expression, which is evaluated and printed in decimal format, with either a leading space or a minus sign ("—"), and one trailing space
- A reference to a string in memory, denoted by '\$' <address>, where <address> is a Factor as usual. Successive memory locations, starting at the specified address, are printed as ASCII characters, until a carriage return (which is not printed) is encountered.

There is no zone spacing in the PRINT statement, nor does NIBL perform an automatic carriage return/line feed after printing 72 characters. NIBL is not an output-oriented language; fancy formatting has been sacrificed for more useful control structures and data manipulation features. (A subroutine to print a number and skip to the next print zone is a trivial to write in NIBL — it takes about two lines of code, with the DO/UNTIL and FOR/NEXT.)

STRING HANDLING STATEMENTS

String handling in NIBL is very minimal and low-level. The string handling features of the INPUT and PRINT statements have already been mentioned; NIBL provides two more statements for manipulating strings.

A statement such as \$<address> = "THIS IS A STRING" would cause the quoted string to be stored in

memory starting at the specified address (which again is a Factor), with a carriage return being appended to the string.

Another statement allows the programmer to move strings around in memory once they have been created. The form of this statement is '\$' <destination> '=' '\$' <source>, where both <destination> and <source> are Factors, and are the addresses of strings in memory. This statement causes all the characters in the string pointed to by <source> to be copied one-by-one to the memory pointed to by <destination>, until a carriage return (also copied) is encountered. Overlapping the source and destination addresses can produce disastrous results, such as wiping out the entire contents of the current page. Consequently, a string move can be aborted by hitting the BREAK key on the teletype (but it must be done quickly!).

Note that all strings referred to in these statements, and in the INPUT and PRINT statements, are assumed to lie within a 4K page, and wraparound is a possibility which must be anticipated by the programmer. (Long-time SC/MP programmers will be familiar with this minor problem.)

Using these statements, it should be very easy to develop a set of NIBL subroutines for performing concatenation, comparison, and substring operations on strings.

END STATEMENT

The END statement may appear anywhere in a NIBL program and not necessarily at the end. It causes a message and the current line number to be printed, with NIBL returning to edit mode. The END statement is useful when debugging programs, since it acts as a breakpoint in the program that can be removed easily.

LINK STATEMENT

The LINK statement allows NIBL programs to call SC/MP machine language routines at any address. A statement of the form 'LINK' <address>, where <address> is an arbitrary expression, will cause the NIBL system to call the routine at that address by executing an appropriate XPPC P3 (Exchange contents of the Program Counter with designated Pointer Register P3) instruction. The user's routine should make sure that it returns by executing another XPPC P3, and that the value of P3 (Pointer Register #3) upon entry to the routine is restored before returning. The routine may make use of the fact that P2 is set by NIBL to point to the beginning of the RAM block used to store the variables A through Z, with each variable being stored low byte first, high byte second. Thus, parameters may be passed between NIBL programs and machine language routines through the variables. Both P1 and P2 may be modified by the user's routines; they are automatically restored by the NIBL system upon return. The user should be careful not to modify RAM locations with negative displacements relative to P2, or the locations with displacements greater than 51 relative to P2. These locations are used by the interpreter.

REMARK STATEMENT

A comment can be inserted into a NIBL program by preceding it with the word REM. REM causes the rest of the line to be ignored by NIBL during execution. Remarks are useful in debugging programs or helping other people to understand them, but of course, they take up valuable memory. (Then again, memory is getting cheaper all the time.)

MULTIPLE STATEMENTS ON ONE LINE

A program line may contain more than one statement, if the statements are separated by colons (":"). Using multiple statements on a single line improves the readability of the program by separating it into small blocks, and uses less memory for storing the program.

It is important to note that an IF statement will cause any statements appearing after it on the line to be ignored if the IF condition turns out to be false. This is the feature that allows a group of statements to be executed conditionally.

A multiple-statement line may be entered without a line number, but NIBL will only execute the first statement on the line, ignoring the rest.

POWERING UP

NIBL is capable of executing a program in ROM in Page 2 immediately upon powering up, without the need for the user to give the RUN command at the teletype. When NIBL initializes, it examines Page 2 and makes an educated guess about the possible existence of a legal NIBL program in that page. If NIBL thinks there really is a program there, it starts executing it immediately; thus, if the program halts for some reason, the value of PAGE will be 2. But if NIBL fails to find a legal program in Page 2 initially, it sets the value of PAGE to 1 (the normal case) and prompts at the teletype.

When executing programs, NIBL periodically checks for keyboard interrupt, returning to edit mode if it detects it. Therefore, if a NIBL program is to be executed with the teletype disconnected, the Sense B line of the SC/MP should be set high so that NIBL will not sense an interrupt while running. This would allow a NIBL system to act as a process controller which starts executing immediately upon powering up.

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INTERFACE AGE 113

SOFTWARE SECTION

MICROCOMPUTER DEVELOPMENT SOFTWARE

```

247 0101 C7FF      LD      @-1(P3)      ;GET HIGH PART OF OLD PC
248 0103 01        XAE
249 0104 C7FF      LD      @-1(P3)      ;GET LOW PART OF OLD PC
250 0106 33        XPAL      P3
251 0107 CAF9      ST      PCSTK(P2)      ;UPDATE IL STACK POINTER
252 0109 40        LD
253 010A 37        XPAH      P3          ;P3 NOW HAS OLD IL PC
254 010B 908E      JMP      CHEAT1
255 010D 9041      EOA:      JMP      E0
256
257
258 ; *****
259 ; *      SAVE GOSUB RETURN ADDRESS      *
260 ; *****
261
262 010F C2FC      SAV:      LD      SBRPTR(P2)
263 0111 E47A      XRI      L(DOSTAK)      ;CHECK FOR MORE
264 0113 981C      JZ      SAV2          ; THAN 8 SAVES
265 0115 AAF6      ILD      SBRPTR(P2)
266 0117 AAF6      ILD      SBRPTR(P2)
267 0119 33        XPAL      P3          ;SET P3 TO
268 011A C410      LDI      H(SBRSTK)      ;SUBROUTINE STACK TOP.
269 011C 37        XPAH      P3
270 011D C2F4      LD      RUNMOD(P2)      ;IF IMMEDIATE MODE,
271 011F 980A      JZ      SAV1          ;SAVE NEGATIVE ADDRESS.
272 0121 35        XPAH      P1          ;SAVE HIGH PORTION
273 0122 CBFF      ST      -1(P3)        ;OF CURSOR
274 0124 35        XPAL      P1
275 0125 31        XPAL      P1          ;SAVE LOW PORTION
276 0126 CBFE      ST      -2(P3)        ;OF CURSOR
277 0128 31        XPAL      P1
278 0129 90C1      JMP      X0          ;RETURN
279 012B C4FF      SAV1:      LDI      -1(P3)      ;IMMEDIATE MODE
280 012D CBFF      ST      -1(P3)        ;RETURN ADDRESS IS
281 012F 90B8      JMP      X0          ;NEGATIVE.
282 0131 C40A      SAV2:      LDI      10       ;ERROR: MORE THAN
283 0133 901B      JMP      E0          ;8 GOSUBS
284
285 ; *****
286 ; *      CHECK STATEMENT FINISHED      *
287 ; *****
288
289
290 0135 C501      DONE:      LD      @1(P1)      ;SKIP SPACES
291 0137 E420      XRI
292 0139 98FA      JZ      DONE          ;
293 013B E42D      XRI      / 1 OD      ;IS IT CARRIAGE RETURN?
294 013D 980A      JZ      DONE1         ;YES - RETURN
295 013F E437      XRI      037         ;IS CHAR A " : " ?
296 0141 9C01      JNZ      DONE2         ;NO - ERROR
297 0143 3F        DONE1:      XPPC      P3      ;YES - RETURN
298 0144 C404      DONE2:      LDI      4
299 0146 9008      JMP      E0
300
301
302 ; *****
303 ; *      RETURN FROM GOSUB      *
304 ; *****
305
306 0148 C2FC      RSTR:      LD      SBRPTR(P2)
307 014A E46A      XRI      L(SBRSTK)      ;CHECK FOR RETURN
308 014C 9C04      JNZ      RSTR1         ;W/O GOSUB.
309 014E C409      LDI      9
310 0150 9043      E0:      JMP      ;GOTO ERROR.
311 0152 BAF6      RSTR1:      LD      SBRPTR(P2)
312 0154 BAF6      DLD      SBRPTR(P2)      ;POP GOSUB STACK,
313 0156 33        XPAL      P3          ;PUT PTR INTO P3.
314 0157 C410      LDI      H(SBRSTK)
315 0159 37        XPAH      P3
316 015A C301      LD      1(P3)        ;IF ADDRESS NEGATIVE,
317 015C 9409      JP      RSTR2         ;SUBROUTINE WAS CALLED
318 015E C402      JS      P3,FIN        ;IN IMMEDIATE MODE,
319 0160 9085      X1:      JMP      X0          ;SO FINISH UP EXECUTING
320 0162 35        RSTR2:      XPAH      P1          ;RESTORE CURSOR HIGH
321 0164 C300      LD      0(P3)
322 0166 31        XPAL      P1          ;RESTORE CURSOR LOW
323 0168 C401      LDI      1          ;SET RUN MODE
324 016D CAF4      ST      RUNMOD(P2)
325 016F 90F4      JMP      X1
326
327 ; *****
328 ; *      TRANSFER TO NEW STATEMENT      *
329 ; *****
330
331
332 0171 C2F2      XFER:      LD      LABLHI(P2)      ;CHECK FOR NON-EXISTENT LINE
333 0173 9404      JP      XFER1         ;
334 0175 C408      LDI      8
335 0177 901C      JMP      E1          ;
336 0179 C401      XFER1:      LDI      1          ;SET RUN MODE TO 1
337 017B CAF4      ST      RUNMOD(P2)
338 017D 3F        XPPC      P3
339
340
341 ; *****
342 ; *      PRINT STRING IN TEXT      *
343 ; *****
344
345 017E          PRS:      LDP1      P3,PUTC-1      ;POINT P3 AT PUTC ROUTINE
346 0184 C501      LD      @1(P1)        ;LOAD NEXT CHAR
347 0186 E422      XRI      / 1         ;IF " ", END OF
348 0188 980B      JZ      X1          ;STRING
349 018A E42F      XRI      02F         ;IF CR, ERROR
350 018C 9805      JZ      PRS1         ;
351 018E E40D      XRI      0D          ;RESTORE CHAR
352 0190 3F        XPPC      P3          ;PRINT CHAR
353 0191 90EB      JMP      PRS          ;GET NEXT CHAR
354 0193 C407      PRS1:      LDI      7          ;SYNTAX ERROR
355 0195 9035      E1:      JMP      E0
356
357 ; *****
358 ; *      PRINT NUMBER ON STACK      *
359 ; *****
360
361 ; THIS ROUTINE IS BASED ON DENNIS ALLISON'S BINARY TO DECIMAL
362 ; CONVERSION ROUTINE IN VOL. 1, #1 OF "DR. DOB'S JOURNAL",
363 ; BUT IS MUCH MORE OBSCURE BECAUSE OF THE STACK MANIPULATION.
364
365
366 ; *****
367 0197 C410      PRN:      LD      H(AESTK)      ;POINT P3 AT A.E. STACK
368 0199 37        XPAH      P3
369 019A AAFD      ILD      LSTK(P2)
370 019C AAFD      ILD      LSTK(P2)
371 019E 33        XPAL      P3
372 019F C40A      LDI      10          ;PUT 10 ON STACK (WE'LL BE
373 01A1 CBFE      ST      -2(P3)        ;DIVIDING BY IT LATER)
374 01A3 C400      LDI      0
375 01A5 CBFF      ST      -1(P3)
376 01A7 C405      LDI      5          ;SET CHNUM TO POINT TO PLACE
377 01A9 CAE7      ST      CHNUM(P2)      ;IN STACK WHERE WE STORE
378 01AB C4FF      LDI      -1          ;THE CHARACTERS TO PRINT
379 01AD CB05      ST      5(P3)          ;FIRST CHAR IS A FLAG (-1)
380 01AF C3FD      LD      -3(P3)        ;CHECK IF NUMBER IS NEGATIVE
381 01B1 9413      JP      $1          ;
382 01B3 C42D      ST      / 1         ;PUT '-' ON STACK, AND NEGATE
383 01B5 CB04      LD      4(P3)        ;THE NUMBER
384 01B7 C400      LDI      0
385 01B9 03        SCL
386 01BA FBFC      CAD      -4(P3)
387 01BC CBFC      ST      -4(P3)
388 01BE C400      LDI      0
389 01C0 FBFD      CAD      -3(P3)
390 01C2 CBFD      ST      -3(P3)
391 01C4 909F      JMP      X1          ;GO DO DIVISION BY 10
392 01C6 C420      $1:      LDI      / 1         ;IF POSITIVE, PUT / ON
393 01C8 CB04      ST      4(P3)        ;STACK BEFORE DIVISION
394 01CA 9099      X4:      JMP      X1
395 01CC 9057      E2:      JMP      ERR1
396
397 ; THE DIVISION IS PERFORMED, THEN CONTROL IS TRANSFERRED
398 ; TO PRN1, WHICH FOLLOWS.
399
400 01CE AAFD      PRN1:      ILD      LSTK(P2)      ;POINT P1 AT A.E. STACK
401 01D0 AAFD      ILD      LSTK(P2)
402 01D2 31        XPAL      P1
403 01D3 C410      LDI      H(AESTK)
404 01D5 35        XPAH      P1
405 01D6 AA67      ILD      CHNUM(P2)      ;INCREMENT CHARACTER STACK
406 01D8 01        XAE
407 01D9 C101      LD      1(P1)        ;POINTER, PUT IN EX. REG.
408 01DB DC30      ORI      0          ;GET REMAINDER FROM DIVIDE.
409 01DD C980      ST      EREG(P1)        ;PUT IT ON THE STACK
410 01DF C1FD      LD      -3(P1)        ;IS THE QUOTIENT ZERO YET?
411 01E1 D9FC      OR      -4(P1)
412 01E3 980A      JZ      $PRNT         ;YES - GO PRINT THE NUMBER
413 01E5 C40F      LDI      H(PNUM1)      ;NO - CHANGE THE I.L. PC
414 01E7 CAF6      ST      PCHIGH(P2)    ;SO THAT DIVIDE IS
415 01E9 C42F      LDI      L(PNUM1)      ;PERFORMED AGAIN
416 01EB CAF8      ST      PCLOW(P2)
417 01ED 90DB      JMP      X4          ;GO DO DIVISION BY 10 AGAIN
418 01EF          $PRNT:      LDP1      P3,PUTC-1      ;POINT P3 AT PUTC ROUTINE
419 01F1 C2F5      LD      LISTNG(P2)    ;IF LISTING, SKIP PRINTING
420 01F3 9C06      JNZ      $2          ;LEADING SPACE
421 01F5 F104      LD      4(P1)        ;PRINT EITHER '-'
422 01F7 3F        XPPC      P3          ;OR LEADING SPACE
423 01F9 C2E7      LD      CHNUM(P2)      ;GET EX. REG. VALUE BACK
424 01FE 01        XAE
425 01FF C580      $2:      LD      @EREG(P1)      ;POINT P3 AT FIRST CHAR
426 0201 C100      LD      P1          ;TO BE PRINTED
427 0203 3F        XPPC      P3          ;PRINT THE CHARACTER
428 0204 C5FF      LD      @-1(P1)      ;GET NEXT CHARACTER
429 0206 94FB      JP      $LOOP        ;REPEAT UNTIL = -1
430 0208 C450      LDI      L(AESTK)
431 020A CAFD      ST      LSTK(P2)      ;CLEAR THE A.E. STACK
432 020C C2F5      LD      LISTNG(P2)    ;PRINT A TRAILING SPACE
433 020E 9CBA      JNZ      X4          ;IF NOT LISTING PROGRAM
434 0210 C420      LDI      / 1
435 0212 3F        XPPC      P3
436 0213 90B5      JMP      X4
437
438 ; *****
439 ; *      CARRIAGE RETURN/LINE FEED      *
440 ; *****
441
442
443 0215          NLINE:      LDP1      P3,PUTC-1      ;POINT P3 AT PUTC ROUTINE
444 021B C40D      LD      OD          ;CARRIAGE RETURN
445 021D 3F        XPPC      P3
446 021E C40A      LD      OA          ;LINE FEED
447 0220 3F        XPPC      P3
448 0221 90A7      X5:      JMP      X4
449
450 ; *****
451 ; *      ERROR ROUTINE      *
452 ; *****
453
454
455          LOCAL
456 0223 C405      ERR:      LDI      5          ;SYNTAX ERROR
457 0225 CAEB      ERR1:      LD      NUM(P2)      ;SAVE ERROR #
458 0227 C2EB      ERR2:      LD      NUM(P2)
459 0229 CAEA      ST      TEMP(P2)
460 022B          LDP1      P3,PUTC-1      ;POINT P3 AT PUTC
461 0231 C40D      LD      OD          ;PRINT CR/LF
462 0233 3F        XPPC      P3
463 0234 C40A      LD      OA
464 0236 3F        XPPC      P3
465 0237          LDP1      P1,MESGS      ;P1 -> ERROR MESSAGES
466 023D BAEB      $1:      LD      NUM(P2)      ;IS THIS THE RIGHT MESSAGE?
467 023F 9806      JZ      $MSG         ;YES - GO PRINT IT
468 0241 C501      $LOOP:      LD      @1(P1)      ;NO - SCAN THROUGH TO
469 0243 94FC      JP      $LOOP        ;NEXT MESSAGE
470 0245 90F6      JMP      $1
471 0247 C501      $MSG:      LD      @1(P1)      ;GET MESSAGE CHAR
472 0249 3F        XPPC      P3          ;PRINT IT
473 024B C1FF      LD      -1(P1)        ;IS MESSAGE DONE?
474 024C 94F9      JP      $MSG         ;NO - GET NEXT CHAR
475 024E C2EA      LD      TEMP(P2)      ;WAS THIS A BREAK MESSAGE?
476 0250 E40E      XRI      14
477 0252 980D      JZ      $3          ;YES - SKIP PRINTING 'ERROR'
478 0254          LDP1      P1,MESGS      ;NO - PRINT 'ERROR'
479 025A C501      $2:      LD      @1(P1)      ;GET CHARACTER
480 025C 3F        XPPC      P3          ;PRINT IT
481 025D C1FF      LD      -1(P1)        ;DONE?
482 025F 94F9      JP      $2          ;NO - REPEAT LOOP
483 0261 C2F4      $3:      LD      RUNMOD(P2)    ;DON'T PRINT LINE #
484 0263 984D      JZ      FIN          ;IF IMMEDIATE MODE
485 0265 C420      LDI      / 1
486 0267 3F        XPPC      P3          ;SPACE
487 0268 C441      LDI      'A'          ;AT
488 026A 3F        XPPC      P3
489 026B C454      LD      'T'
490 026D 3F        XPPC      P3
491 026E C410      LD      H(AESTK)      ;POINT P3 AT A.E. STACK
492 0270 37        XPAH      P3
493 0271 AAFD      ILD      LSTK(P2)
494 0273 AAFD      ILD      LSTK(P2)
495 0275 33        XPAL      P3
496 0277 C2F7      LD      H(LINE(P2))      ;GET HIGH BYTE OF LINE #
497 0279 CBFF      LD      -1(P3)        ;PUT ON STACK
498 027A C2F8      LD      L(LINE(P2))      ;GET LOW BYTE OF LINE #
499 027C CBFE      ST      -2(P3)        ;PUT ON STACK
500 027E C42D      LD      L(ERNUM)      ;GO TO PRN
501 0280 CAF8      ST      PCLOW(P2)
502 0282 C40E      LD      H(ERNUM)
503 0284 CAF8      ST      PCHIGH(P2)
504 0286 9099      X5A:      JMP      X5
505
506 ; *****
507 ; *      BREAK, NXT, FIN, & STRT      *
508 ; *****
509
510

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511 0288 C40E BREAK: LDI 14
512 028A 9099 E3A: JMP ERR1
513
514 028C C2F4 NXT: LD RUNMOD(P2) ; *** NEXT STATEMENT ***
515 028E 9822 JZ FIN ; IF IN IMMED. MODE,
516 0290 C100 LD (P1) ; STOP EXECUTION
517 0292 D480 ANI 080 ; IF WE HIT END OF FILE,
518 0294 9C1C JNZ FIN ; FINISH UP THINGS
519 0296 06 CSA
520 0297 D420 ANI 020 ; BREAK IF SOMEONE IS
521 0299 98ED JZ BREAK ; TYPING ON THE CONSOLE
522 029B C1FF LD -1(P1) ; GET LAST CHARACTER SCANNED
523 029D E40D XRI 0D ; WAS IT CARRIAGE RETURN?
524 029F 9C08 JNZ NXT1 ; YES - SKIP FOLLOWING UPDATES
525 02A1 C501 LD 01(P1) ; GET HIGH BYTE OF NEXT LINE #
526 02A3 CAF7 ST HILINE(P2) ; SAVE IT
527 02A5 C502 ST LLINE(P2) ; GET LOW BYTE OF LINE #, SKIP
528 02A7 CAF8 LD L(STMT) ; LINE LENGTH BYTE
529 02A9 C40C NXT1: LDI H(STMT) ; GO TO 'STMT' IN IL TABLE
530 02AB CAF4 ST PCHIGH(P2)
531 02AD C482 LDI L(STMT)
532 02AF CAFB ST PCLOW(P2)
533 02B1 3F XPPC P3
534
535 02B2 C400 FIN: LDI 0 ; *** FINISH EXECUTION ***
536 02B4 CAF4 ST RUNMOD(P2) ; CLEAR RUN MODE
537 02B6 C450 LD L(AESTK) ; CLEAR ARITHMETIC STACK
538 02B8 CAFD ST LSTK(P2)
539 02BA C418 LDI L(START) ; SET IL PC TO GETTING LINES
540 02BC CAFB ST PCLOW(P2)
541 02BE C40C LDI H(START)
542 02C0 CAF4 ST PCHIGH(P2)
543 02C2 C4A6 LDI L(PCSTAK)
544 02C4 CAF9 ST PCSTK(P2)
545 02C6 90BE JMP X5A
546
547 02C8 AAF4 STRT: ILD RUNMOD(P2) ; *** START EXECUTION ***
548 02CA C2E9 LD TEMP2(P2) ; RUN MODE = 1
549 02CC 35 P1 XPAH ; POINT CURSOR TO
550 02CD C2E8 P1 TEMP3(P2) ; START OF NIBL PROGRAM
551 02CF 31 XPAL P1
552 02D0 C46A LDI L(SBRSTK) ; EMPTY SOME STACKS:
553 02D2 CAFD ST SBRPTR(P2) ; GOSUB STACK,
554 02D4 C48A LDI L(FORSTK)
555 02D6 CAFD ST FORPTR(P2) ; FOR STACK
556 02D8 C47A LDI L(DOSTAK)
557 02DA CAFD ST DOSTPTR(P2) ; & DO/UNTIL STACK
558 02DC 3F XPPC P3 ; RETURN
559 02DD 90A7 X6: JMP X5A
560 02DF 90A9 E4: JMP E3A
561
562
563 ; *****
564 ; * LIST NIBL PROGRAM *
565 ; *****
566
567 02E1 C100 LST: LD (P1) ; CHECK FOR END OF FILE
568 02E3 E480 XRI 080
569 02E5 9418 JP LST2
570 02E7 C410 LDI H(AESTK) ; GET LINE NUMBER ONTO STACK
571 02E9 37 XPAH P3
572 02EA AAFD ILD LSTK(P2)
573 02EC AAFD ILD LSTK(P2)
574 02EE 33 XPAL P3
575 02EF C501 LD 01(P1)
576 02F1 CBFF ST -1(P3)
577 02F3 C501 LD 01(P1)
578 02F5 CBFE ST -2(P3)
579 02F7 C501 LD 01(P1) ; SKIP OVER LINE LENGTH
580 02F9 C401 LDI 1
581 02FB CAF5 ST LISTNG(P2) ; SET LISTING FLAG
582 02FD 90DE JMP X6 ; GO PRINT LINE NUMBER
583 02FF C400 LST2: LDI 0
584 0301 CAF5 ST LISTNG(P2) ; CLEAR LISTING FLAG
585 0303 C402 JS P3,NXT ; GO TO NXT
586 030A 90D1 X6A: JMP X6
587 030C 90D1 E5: JMP E4
588 030E LST3: LDI P3,PUTC-1 ; POINT P3 AT PUTC
589 0314 06 LST4: CSA
590 0315 D420 ANI 020
591 0317 98E6 JZ LST2 ; IF TYPING, STOP
592 0319 C501 LD 01(P1) ; GET NEXT CHAR
593 031B E40D XRI 0D ; TEST FOR CR
594 031D 9805 JZ LST5
595 031F E40D XRI 0D ; GET CHARACTER
596 0321 3F XPPC P3 ; PRINT CHARACTER
597 0322 90F0 JMP LST4
598 0324 C40D LST5: LDI 0D ; CARRIAGE RETURN
599 0326 3F XPPC P3
600 0327 C40A LDI 0A ; LINE FEED
601 0329 3F XPPC P3
602 032A 02 CCL
603 032B C447 LDI L(LIST3)
604 032D CAFB ST PCLOW(P2)
605 032F C40C LDI H(LIST3)
606 0331 CAF4 ST PCHIGH(P2)
607 0333 90AC JMP LST ; GET NEXT LINE
608
609
610 ; *****
611 ; * ADD AND SUBTRACT *
612 ; *****
613
614 0335 C410 ADD: LDI H(AESTK) ; SET P3 TO CURRENT
615 0337 37 XPAH P3 ; STACK LOCATION
616 0338 BAFD DLD LSTK(P2)
617 033A BAFD DLD LSTK(P2)
618 033C 33 XPAL P3
619 033D 02 CCL
620 033E C3FE LD -2(P3) ; REPLACE TWO TOP ITEMS
621 0340 F300 ADD 0(P3) ; ON STACK BY THEIR SUM
622 0342 CBFE ST -2(P3)
623 0344 C3FF LD -1(P3)
624 0346 F301 ADD 1(P3)
625 0348 CBFF ST -1(P3)
626 034A 90BE X7: JMP X6A
627
628 034C C410 SUB: LDI H(AESTK) ; SET P3 TO CURRENT
629 034E 37 XPAH P3 ; STACK LOCATION
630 034F BAFD DLD LSTK(P2)
631 0351 BAFD DLD LSTK(P2)
632 0353 33 XPAL P3
633 0354 03 SCL
634 0355 C3FE LD -2(P3) ; REPLACE TWO TOP ITEMS
635 0357 FB00 CAD 0(P3) ; ON STACK BY THEIR DIFFERENC
636 0359 CBFE ST -2(P3)
637 035B C3FF LD -1(P3)
638 035D FB01 CAD 1(P3)
639 035F CBFF ST -1(P3)
640 0361 90A7 JMP X6A
641
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643

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778 0439 90B4 X9A: JMP X9
779 043B C3FD LD -3(P3) ;STORE NON-NEGATED DIVIDEND
780 043D C602 ST 2(P3) ; IN 32-BIT ACCUMULATOR
781 043F C3FC ST -4(P3)
782 0441 C602 ST 3(P3)
783 0443 C3FF $1: LD -1(P3) ;CHECK FOR NEGATIVE DIVISOR
784 0445 940D JF $2
785 0447 C400 LDI 0 ;NEGATE DIVISOR
786 0449 03 SCL
787 044A FBFE CAD -2(P3)
788 044C CBFE ST -2(P3)
789 044E C400 LDI 0
790 0450 FBFF CAD -1(P3)
791 0452 C3FF ST -1(P3)
792 0454 C400 $2: LDI 0 ;PUT ZERO IN:
793 0456 CB01 ST 1(P3) ; LEFT HALF OF 32-BIT ACC.
794 0458 CB00 ST 0(P3)
795 045A CAEB ST NUM(P2) ; THE COUNTER, AND
796 045C CBFD ST -3(P3) ; IN THE DIVIDEND, NOW USED
797 045E CBFC ST -4(P3) ; STORE THE QUOTIENT
798 0460 02 $LOOP: CCL ;BEGIN MAIN DIVIDE LOOP:
799 0461 C3FC LD -4(P3) ; SHIFT QUOTIENT LEFT,
800 0463 F3FC ADD -4(P3)
801 0465 CBFC ST -4(P3)
802 0467 C3FD LD -3(P3)
803 0469 F3FD ADD -3(P3)
804 046B CBFD ST -3(P3)
805 046D 02 CCL ; SHIFT 32-BIT ACC LEFT,
806 046E C303 LD 3(P3)
807 0470 F303 ADD 3(P3)
808 0472 CB03 ST 3(P3)
809 0474 C302 LD 2(P3)
810 0476 F302 ADD 2(P3)
811 0478 CB02 ST 2(P3)
812 047A C301 LD 1(P3)
813 047C F301 ADD 1(P3)
814 047E CB01 ST 1(P3)
815 0480 C300 LD (P3)
816 0482 F300 ADD (P3)
817 0484 CB00 ST (P3)
818 0486 03 SCL
819 0487 C301 LD 1(P3) ; SUBTRACT DIVISOR INTO
820 0489 FBFE CAD -2(P3) ; LEFT HALF OF ACC.
821 048B CB01 ST 1(P3)
822 048D C300 LD (P3)
823 048F FBFF CAD -1(P3)
824 0491 CB00 ST (P3)
825 0493 9411 JF $ENT1
826 0495 02 CCL
827 0496 C301 LD 1(P3)
828 0498 F3FE ADD -2(P3)
829 049A CB01 ST 1(P3)
830 049C C300 LD (P3)
831 049E F3FF ADD -1(P3)
832 04A0 CB00 ST (P3)
833 04A2 900B $3: JMP $3
834 04A4 9093 X9B: JMP X9A
835 04A6 C3FC $ENT1: LD -4(P3) ; ELSE IF RESULT POSITIVE,
836 04A8 DC01 ORI 1 ; RECORD A 1 IN QUOTIENT
837 04AA CBFC ST -4(P3) ; W/O RESTORING THE ACC
838 04AC AAE8 LD NUM(P2) ; INCREMENT THE COUNTER
839 04AE E410 XRI 16 ; ARE WE DONE?
840 04B0 9CAE JNZ $LOOP
841 04B2 C2EA LD TEMP(P2) ; LOOP IF NOT DONE
842 04B4 940D JF $END
843 04B6 C400 LDI 0 ; CHECK THE QUOTIENT'S SIGN,
844 04B8 03 SCL ; NEGATING IF NECESSARY
845 04B9 FBFC CAD -4(P3)
846 04BB CBFC ST -4(P3)
847 04BD C400 LDI 0
848 04BF FBFD CAD -3(P3)
849 04C1 CBFD ST -3(P3)
850 04C3 BA05 DLD LSTK(P2) ; DECREMENT THE STACK POINTER,
851 04C5 BA0D DLD LSTK(P2) ; AND EXIT
852 04C7 90DB JMP X9B
853
854
855 ; *****
856 ; * STORE VARIABLE *
857 ; *****
858
859 04C9 C410 STORE: LDI H(AESTK) ;SET P3 TO STACK
860 04CB 37 XPAH P3
861 04CD C2FD LD LSTK(P2)
862 04CE 33 XPAL P3
863 04CF C7FD LD E-3(P3) ;GET VARIABLE INDEX
864 04D1 01 XAE ;PUT IN E REG
865 04D2 C301 LD 1(P3)
866 04D4 CA80 ST EREG(P2) ;STORE LOWER 8 BITS
867 04D6 02 CCL ; INTO VARIABLE
868 04D7 40 LDE 1 ;INCREMENT INDEX
869 04D8 F401 RAL
870 04DA 01 XAE
871 04DB C302 LD 2(P3)
872 04DD CA80 ST EREG(P2) ;STORE UPPER 8 BITS
873 04DF 33 XPAL P3 ; INTO VARIABLE
874 04E0 CAFD ST LSTK(P2) ; UPDATE STACK POINTER
875 04E2 C400 X10: JS P3,EXECIL
876
877
878 ; *****
879 ; * TEST FOR VARIABLE IN TEXT *
880 ; *****
881
882 04E9 C501 TSTVAR: LD @1(P1)
883 04EB E420 XRI ;SLEW OFF SPACES
884 04ED 98FA JZ TSTVAR
885 04EF C1FF LD -1(P1) ;GET CHARACTER IN QUESTION
886 04F1 03 SCL
887 04F2 FC5B CAI 'Z'+1 ;SUBTRACT 'Z'+1
888 04F4 9405 JF *FAIL ;NOT VARIABLE IF POSITIVE
889 04F6 03 SCL
890 04F7 FCE6 CAI 'A'-'Z'-1 ;SUBTRACT 'A'
891 04F9 9412 JF *MAYBE ;IF POS, MAY BE VARIABLE
892 04FB C5FF LD -1(P1) ;BACKSPACE CURSOR
893 04FD C2FB DLD PCLOW(P2) ;GET TEST-FAIL ADDRESS
894 04FF 33 XPAL P3 ; FROM I.L. TABLE, PUT IT
895 0500 C2FA LD PCHIGH(P2) ; INTO I.L. PROGRAM COUNTER
896 0502 37 XPAH P3
897 0503 C300 LD (P3)
898 0505 CAFA ST PCHIGH(P2)
899 0507 C301 LD 1(P3)
900 0509 CAFB ST PCLOW(P2)
901 050B 9005 JMP X10
902 050D 01 $MAYBE: XAE ;SAVE VALUE (0-25)
903 050E C100 LD (P1) ;CHECK FOLLOWING CHAR
904 0510 03 SCL ;MUST NOT BE A LETTER
905 0511 FC5B CAI 'Z'+1 ; OTHERWISE WE'D BE LOOKING
906 0513 9405 JF *OK ; AT A KEYWORD, NOT VARIABLE
907 0515 03 SCL
908 0516 FCE6 CAI 'A'-'Z'-1
909 0518 94E1 JF *FAIL
910 051A C410 $OK: LDI H(AESTK) ;SET P3 TO CURRENT
911 051C 37 XPAH P3 ; STACK LOCATION
912 051D AAFD ILD LSTK(P2) ; INCR STACK POINTER
913 051F 33 XPAL P3
914 0520 02 CCL
915 0521 40 LDE
916 0522 70 ADE
917 0523 CBFF ST -1(P3) ;PUT INDEX ON STACK
918 0525 CA02 LDI 2 ;INCREMENT I.L. PC, SKIPPING
919 0527 02 CCL ; OVER TEST-FAIL ADDRESS
920 0528 F2FB ADD PCLOW(P2)
921 052A CAFB ST PCLOW(P2)
922 052C C400 LDI 0
923 052E F2FA ADD PCHIGH(P2)
924 0530 CAFA ST PCHIGH(P2)
925 0532 90AE JMP X10
926
927
928 ; *****
929 ; * IND -- EVALUATE A VARIABLE *
930 ; *****
931
932 0534 C410 IND: LDI H(AESTK) ;SET P3 TO STACK
933 0536 37 XPAH P3
934 0537 AAFD ILD LSTK(P2)
935 0539 33 XPAL P3
936 053A CBFE LD -2(P3) ;GET INDEX OFF TOP
937 053C 01 XAE ;PUT INDEX IN E REG
938 053D C280 LD EREG(P2) ;GET LOWER 8 BITS
939 053F CBFE ST -2(P3) ;SAVE ON STACK
940 0541 02 CCL
941 0542 40 LDE ;INCREMENT E REG
942 0543 F401 ADI 1
943 0545 01 XAE
944 0546 C280 LD EREG(P2) ;GET UPPER 8 BITS
945 0548 CBFF ST -1(P3) ;SAVE ON STACK
946 054A 9096 X11: JMP X10
947
948 ; *****
949 ; * RELATIONAL OPERATORS *
950 ; *****
951
952
953 054C C401 EQ: LDI 1 ;EACH RELATIONAL OPERATOR
954 054E 9012 JMP CMP ;LOADS A NUMBER USED LATER
955 0550 C402 NEO: LDI 2 ;AS A CASE SELECTOR, AFTER
956 0552 900E JMP CMP ;THE TWO OPERANDS ARE COM-
957 0554 C403 LSS: LDI 3 ;PARED. BASED ON THE COM-
958 0556 900A JMP CMP ;PARISON, FLAGS ARE SET THAT
959 0558 C404 LEQ: LDI 4 ;ARE EQUIVALENT TO THOSE SET
960 055A 9006 JMP CMP ;BY THE 'CMP' INSTRUCTION IN
961 055C C405 GTR: LDI 5 ;THE PDP-11. THESE PSEUDO-
962 055E 9002 JMP CMP ;FLAGS ARE USED TO DETERMINE
963 0560 C406 GEQ: LDI 6 ;WHETHER THE PARTICULAR
964 ; RELATION IS SATISFIED OR NO
965 0562 CAEB CMP: ST NUM(P2)
966 0564 C410 LDI H(AESTK) ;SET P3 -> ARITH STACK
967 0566 37 XPAH P3
968 0567 BA0D DLD LSTK(P2)
969 0569 BA0D DLD LSTK(P2)
970 056B 33 XPAL P3
971 056C 03 SCL
972 056D CBFE LD -2(P3) ;SUBTRACT THE TWO OPERANDS,
973 056F FB00 CAD (P3) ;STORING RESULT IN LO & HI
974 0571 CAEF ST LO(P2)
975 0573 C3FF LD -1(P3)
976 0575 FB01 CAD 1(P3)
977 0577 CAEE ST HI(P2)
978 0579 E3FF XOR -1(P3) ;OVERFLOW OCCURS IF SIGNS OF
979 057B 01 XAE ;DIFFER AND SIGNS OF THE
980 057C C3FF LD -1(P3) ;TWO OPERANDS DIFFER
981 057E E301 XOR 1(P3) ;BIT 7 EQUIVALENT TO V FLAG
982 0580 50 ANE ;BIT 7 EQUIVALENT TO N XOR V
983 0581 E2EE XOR HI(P2) ;STORE IN TEMP
984 0583 CAEA ST TEMP(P2)
985 0585 C2EE LD HI(P2) ;Determine IF RESULT WAS ZERO
986 0587 DAFF OR LO(P2)
987 0589 9802 SETZ ;IF RESULT=0, SET Z FLAG
988 058B C480 LDI 080 ;ELSE CLEAR Z FLAG
989 058D E480 SETZ: XRI 080
990 058F 01 XAE ;BIT 7 OF EX = Z FLAG
991
992 0590 BAEB DLD NUM(P2) ;TEST FOR =
993 0592 9C05 JNZ NE01
994 0594 40 LDE ;EQUAL IF Z = 1
995 0595 902B JMP CMP1
996 0597 90B1 X12: JMP X11
997 0599 BAEB NEO1: DLD NUM(P2) ;TEST FOR <
998 059B 9C05 JNZ LSS1
999 059D 40 LDE ;NOT EQUAL IF Z = 0
1000 059E E480 XRI 080
1001 05A0 9020 JMP CMP1
1002 05A2 BAEB LSS1: DLD NUM(P2) ;TEST FOR <
1003 05A4 9C04 LDI LE01
1004 05A6 C2EA LD TEMP(P2) ;LESS THAN IF (N XOR V)=1
1005 05A8 9018 JMP CMP1
1006 05AA BAEB LE01: DLD NUM(P2) ;TEST FOR <=
1007 05AC 9C05 JNZ GTR1
1008 05AE 40 LDE ;LESS THAN OR EQUAL
1009 05AF DAFA OR TEMP(P2) ;IF (Z OR (N XOR V))=1
1010 05B1 900F JMP CMP1
1011 05B3 98EB GTR1: DLD NUM(P2) ;TEST FOR >
1012 05B5 9C07 JNZ GE01
1013 05B7 40 LDE ;GREATER THAN
1014 05B8 DAFA OR TEMP(P2) ;IF (Z OR (N XOR V))=0
1015 05BA E480 XRI 080
1016 05BC 9004 JMP CMP1
1017 05BE C2EA GE01: LD TEMP(P2) ;GREATER THAN OR EQUAL
1018 05C0 E480 XRI 080 ;IF (N XOR V)=0
1019 05C2 C2A4 CMP1: JF FALSE ;IS RELATION SATISFIED?
1020 05C4 C401 LDI 1 ;YES - PUSH 1 ON STACK
1021 05C6 9002 JMP CMP2
1022 05C8 C400 FALSE: LDI 0 ;NO - PUSH 0 ON STACK
1023 05CA CBFE CMP2: ST -2(P3)
1024 05CC C400 LD 0
1025 05CE CBFF ST -1(P3)
1026 05D0 C400 JS P3,RTN ;DO AN I.L. RETURN
1027 05D7 90BE JMP X12
1028
1029 ; *****
1030 ; * IF STATEMENT TEST FOR ZERO *
1031 ; *****
1032
1033
1034 05D9 C2EF CMPR: LD LO(P2) ;GET LOW & HI BYTES OF EXPR.
1035 05DB DAEE OR HI(P2) ;TEST IF EXPRESSION IS ZERO
1036 05DD 9802 JZ FAIL ;YES - IT IS
1037 05DF 9066 JMP X12 ;NO - IT ISN'T SO CONTINUE
1038 05E1 C501 FAIL: LD @1(P1) ;SKIP TO NEXT LINE IN PROGRAM
1039 05E3 E40D XRI 00 ; (I.E. TIL NEXT CR)
1040 05E5 9CFA JNZ FAIL
1041 05E7 F402 JS P3,NXT ;CALL NXT AND RETURN
1042 05EE 90A7 X12A: JMP X12
1043
1044 ; *****
1045 ; * AND, OR, & NOT *
1046 ; *****

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SOFTWARE SECTION

MICROCOMPUTER DEVELOPMENT SOFTWARE

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1047      , *****
1048
1049      LOCAL
1050 05F0 C401 ANDOP: LDI 1 ; EACH OPERATION HAS ITS
1051 05F2 9005 JUMP $1 ; OWN CASE SELECTOR.
1052 05F4 C402 OROP: LDI 2
1053 05F6 9002 JUMP $1
1054 05F8 C403 NOTOP: LDI 3
1055 05FA CAEB $1: ST NUM(P2)
1056 05FC C410 LDI H(AESTK) ; SET P3 -> ARITH. STACK
1057 05FE 37 XPAH P3
1058 05FF B4FD DLD LSTK(P2)
1059 0601 B4FD DLD LSTK(P2)
1060 0603 33 XPAH P3
1061 0604 BAEB DLD NUM(P2) ; TEST FOR 'AND'
1062 0606 900E JNZ $0R
1063 0608 C301 LD 1(P3) ; REPLACE TWO TOP ITEMS ON
1064 060A D3FF AND -1(P3) ; STACK BY THEIR 'AND'
1065 060C CBFF ST -1(P3)
1066 060E C300 LD 0(P3)
1067 0610 D3FE AND -2(P3)
1068 0612 CBFE ST -2(P3)
1069 0614 90D8 JUMP X12A
1070 0616 BAEB DLD NUM(P2) ; TEST FOR 'OR'
1071 0618 900E JNZ $NOT
1072 061A C301 LD 1(P3) ; REPLACE TWO TOP ITEMS ON
1073 061C DBFF OR -1(P3) ; STACK BY THEIR 'OR'
1074 061E CBFF ST -1(P3)
1075 0620 C300 LD 0(P3)
1076 0622 DBFE OR -2(P3)
1077 0624 CBFE ST -2(P3)
1078 0626 90C6 JUMP X12A
1079 0628 C701 LD $1(P3) ; 'NOT' OPERATION
1080 062A E4FF XRI OFF
1081 062C CBFF ST -1(P3) ; REPLACE TOP ITEM ON STACK
1082 062E C701 LD $1(P3) ; BY ITS ONE'S COMPLEMENT
1083 0630 E4FF XRI OFF
1084 0632 CBFF ST -1(P3)
1085 0634 33 XPAH P3
1086 0636 CAFD ST LSTK(P2) ; STACK POINTER FIXUP
1087 0637 90B5 X12B: JUMP X12A
1088
1089 ; *****
1090 ; * EXCHANGE CURSOR WITH RAM *
1091 ; *****
1092
1093 XCHGP1: LD P1LOW(P2) ; THIS ROUTINE IS HANDY WHEN
1094 0639 C2F1 XPAH P1 ; EXECUTING AN 'INPUT' STMT
1095 063B 31 ST P1LOW(P2) ; IT EXCHANGES THE CURRENT
1096 063C CAF1 LD P1HIGH(P2) ; TEXT CURSOR WITH ONE SAVED
1097 063E C2F0 XPAH P1 ; IN RAM
1098 0640 35 ST P1HIGH(P2)
1099 0641 CAF0 XPPC P3
1100 0643 3F
1101
1102 ; *****
1103 ; * CHECK RUN MODE *
1104 ; *****
1105
1106 CKMODE: LD RUNMOD(P2) ; THIS ROUTINE CAUSES AN ERROR
1107 0644 C2F4 JZ CK1 ; IF CURRENTLY IN EDIT MODE
1108 0646 9801 CK1: LD 3
1109 0648 3F CK1: ST NUM(P2) ; ERROR IF RUN MODE = 0
1110 0649 C403 E8: ST P3.ERR2 ; MINOR KLUGE
1111 064B CAEB JS
1112 064D C402
1113
1114 ; *****
1115 ; * GET HEXADECEMAL NUMBER *
1116 ; *****
1117
1118 LOCAL
1119
1120 0654 AAFD HEX: LLD LSTK(P2) ; POINT P3 AT ARITH STACK
1121 0656 AAFD LLD LSTK(P2)
1122 0658 33 XPAH P3
1123 0659 C410 LDI H(AESTK)
1124 065B 37 XPAH P3
1125 065C C400 LDI 0 ; NUMBER INITIALLY ZERO
1126 065E CBFF ST -1(P3) ; PUT IT ON STACK
1127 0660 CBFE ST -2(P3)
1128 0662 CAEB ST NUM(P2) ; ZERO NUMBER OF DIGITS
1129 0664 C501 $SKIP: LD $1(P1) ; SKIP ANY SPACES
1130 0666 E420 XRI
1131 0668 98FA JZ $SKIP
1132 066A C5FF LD $-1(P1) ; GET A CHARACTER
1133 066C C100 $LOOP: LD (P1)
1134 066E 03 SCL
1135 066F FC3A CAI '9'+1 ; CHECK FOR A NUMERIC CHAR
1136 0671 9409 JP $LETR
1137 0673 03 SCL
1138 0674 FCF6 CAI '0'-'9'-1 ; IF NUMERIC, SHIFT NUMBER
1139 0676 9413 JP $ENTER ; AND ADD NEW HEX DIGIT
1140 0678 9032 JMP $END
1141 067A 90BB X12C: JMP X12B
1142 067C 03 $LETR: SCL
1143 067D FC0D CAI '0'-'9'-1 ; CHECK FOR HEX LETTER
1144 067F 942B JP $END
1145 0681 03 SCL
1146 0682 FCFA CAI 'A'-'G'
1147 0684 9402 JP $OK
1148 0686 9024 JMP $END
1149 0688 02 $OK: CCL
1150 0689 F40A ADD 10 ; ADD 10 TO GET TRUE VALUE
1151 068B 01 $ENTER: XAE 4 ; OF LETTER
1152 068C C404 LDI 4 ; NEW DIGIT IN EX REG
1153 068E CAEA ST TEMP(P2) ; SET SHIFT COUNTER
1154 0690 CAEB ST NUM(P2) ; DIGIT COUNT IS NON-ZERO
1155 0692 C3FE $SHIFT: LD -2(P3) ; SHIFT NUMBER LEFT BY 4
1156 0694 02 CCL
1157 0695 F3FE ADD -2(P3)
1158 0697 CBFE ST -2(P3)
1159 0699 C3FF LD -1(P3)
1160 069B F3FF ADD -1(P3)
1161 069D CBFF ST -1(P3)
1162 069F B4EA DLD TEMP(P2)
1163 06A1 9CEA JNZ $SHIFT
1164 06A3 C3FE LD -2(P3) ; ADD NEW DIGIT
1165 06A5 58 ORE ; INTO NUMBER
1166 06A6 CBFE ST -2(P3)
1167 06A8 C501 LD $1(P1) ; ADVANCE THE CURSOR
1168 06AA 90C0 JMP $LOOP ; GET NEXT CHAR
1169 06AC C2EB LD NUM(P2) ; CHECK IF THERE WERE
1170 06AE 9C87 JNZ X12B ; MORE THAN 0 CHARACTERS
1171 06B0 C405 LDI 5 ; ERROR IF THERE WERE NONE
1172 06B2 9097 E8B: JMP E8
1173
1174 ; *****
1175 ; * TEST FOR NUMBER IN TEXT *
1176 ; *****
1177
1178 ; THIS ROUTINE TESTS FOR A NUMBER IN THE TEXT. IF NO
1179 ; NUMBER IS FOUND, I.L. CONTROL PASSES TO THE ADDRESS
1180
1181 ; INDICATED IN THE 'TSTN' INSTRUCTION. OTHERWISE, THE
1182 ; NUMBER IS SCANNED AND PUT ON THE ARITHMETIC STACK,
1183 ; WITH I.L. CONTROL PASSING TO THE NEXT INSTRUCTION.
1184
1185 LOCAL
1186 06B4 C501 TSTNUM: LD $1(P1)
1187 06B6 E420 XRI
1188 06B8 98FA JZ
1189 06BA C5FF LD
1190 06BC 03 SCL
1191 06BD FC3A CAI
1192 06BF 9405 JP
1193 06C1 03 SCL
1194 06C2 FCF6 CAI
1195 06C4 9421 JP $1
1196 06C6 C2FB $ABORT: LD PCLOW(P2) ; GET TEST-FAIL ADDRESS
1197 06C8 33 XPAL P3 ; FROM I.L. TABLE
1198 06C9 C2FA LD PCHIGH(P2)
1199 06CB 37 XPAH P3
1200 06CC C300 LD (P3) ; PUT TEST-FAIL ADDRESS
1201 06CE CAFD ST PCHIGH(P2) ; INTO I.L. PC
1202 06D0 C301 LD 1(P3)
1203 06D2 CAFB JMP PCLOW(P2)
1204 06D4 90A4 LDI X12C
1205 06D6 C402 $RET: CCL 2 ; SKIP OVER ONE IL INSTRUCTION
1206 06D8 02 ; IF NUMBER IS DONE
1207 06D9 F2FB ADD PCLOW(P2)
1208 06DB CAFB ST PCLOW(P2)
1209 06DD C400 LDI 0
1210 06DF F2FA ADD PCHIGH(P2)
1211 06E1 CAFD ST PCHIGH(P2)
1212 06E3 9095 JMP X12C
1213 06E5 90CB E8A: JMP E8B
1214 06E7 01 $1: XAE
1215 06E8 C410 LDI H(AESTK) ; SAVE DIGIT IN EX REG
1216 06EA 37 XPAH P3 ; POINT P3 AT AE STACK
1217 06EB AAFD LLD LSTK(P2)
1218 06ED AAFD LLD LSTK(P2)
1219 06EF 33 XPAL P3
1220 06F0 C400 LDI 0
1221 06F2 CBFF ST -1(P3)
1222 06F4 40 LDE
1223 06F5 CBFE ST -2(P3)
1224 06F7 C501 $LOOP: LD $1(P1) ; GET NEXT CHAR
1225 06F9 C100 LD (P1)
1226 06FB 03 SCL
1227 06FC FC3A CAI '9'+1 ; TEST IF IT IS DIGIT
1228 06FE 94D6 JP $RET ; RETURN IF IT ISN'T
1229 0701 FCF6 CAI '0'-'9'-1
1230 0703 9402 JP $2
1231 0705 90C6 JMP $RET
1232 0707 01 $2: XAE
1233 0708 C3FF LD -1(P3) ; SAVE DIGIT
1234 070A C801 ST 1(P3) ; PUT RESULT IN SCRATCH SPACE
1235 070C C3FE LD -2(P3)
1236 070E C800 ST (P3)
1237 0710 C402 LDI 2
1238 0712 CAEA ST TEMP(P2) ; MULTIPLY RESULT BY 10
1239 0714 02 $SHIFT: CCL ; FIRST MULTIPLY BY 4
1240 0715 C3FE LD -2(P3)
1241 0717 F3FE ADD -2(P3)
1242 0719 CBFE ST -2(P3)
1243 071B C3FF LD -1(P3)
1244 071D F3FF ADD -1(P3)
1245 071F CBFF ST -1(P3)
1246 0721 BAEA DLD TEMP(P2)
1247 0723 9CEA JNZ $SHIFT
1248 0725 02 CCL
1249 0727 C3FE LD -2(P3) ; THEN ADD OLD RESULT,
1250 0729 F300 ADD (P3) ; SO WE HAVE RESULT * 5
1251 072B CBFE ST -2(P3)
1252 072D C3FF LD -1(P3)
1253 072F F301 ADD 1(P3)
1254 0731 CBFF ST -1(P3)
1255 0733 02 CCL
1256 0735 C3FE LD -2(P3) ; THEN MULTIPLY BY TWO
1257 0737 F3FE ADD -2(P3)
1258 0739 CBFE ST -2(P3)
1259 073B C3FF LD -1(P3)
1260 073D F3FF ADD -1(P3)
1261 073F CBFF ST -1(P3)
1262 0741 02 CCL
1263 0743 F301 LD -2(P3) ; THEN ADD IN NEW DIGIT
1264 0745 40 LDE
1265 0747 F3FE ADD -2(P3)
1266 0749 CBFE ST -2(P3)
1267 074B C400 LDI 0
1268 074D F3FF ADD -1(P3)
1269 074F CBFF ST -1(P3)
1270 0751 94AA JP $LOOP ; REPEAT IF NO OVERFLOW
1271 0753 C406 LDI 6
1272 0755 9094 E9: JMP E8A ; ELSE REPORT ERROR
1273 0757 9090 X14: JMP X13
1274
1275 ; *****
1276 ; * GET LINE FROM TELETYPE *
1277 ; *****
1278
1279 LOCAL
1280
1281 0753 LDPI P1.LBUF ; SET P1 TO LBUF
1282 0755 C400 LDI 0 ; CLEAR NO. OF CHAR
1283 0757 CAE7 ST CHNUM(P2)
1284 0759 LDPI P3.PUTC-1 ; POINT P3 AT PUTC ROUTINE
1285 0763 C2F4 LD RUNMOD(P2) ; PRINT '?' IF RUNNING
1286 0765 9808 JZ $0 ; (I.E. DURING 'INPUT')
1287 0767 C43F LD '?'
1288 0769 3F XPPC P3
1289 076A C420 LDI
1290 076C 3F XPPC P3
1291 076D 9003 JMP $1
1292 076F C43E LD '0' ; OTHERWISE PRINT '0'
1293 0771 3F XPPC P3
1294 0772 C40F $1: JS P3.GECO ; GET CHARACTER
1295 0774 C4BD LDI L(PUTC)-1 ; POINT P3 AT PUTC AGAIN
1296 0776 33 XPAL P3
1297 077C 40 LDE
1298 077D 98F3 JZ $1 ; GET TYPED CHAR
1299 077F E40A XRI 0A ; IGNORE NULLS
1300 0781 98EF JZ $1 ; IGNORE LINE FEED
1301 0783 40 LDE
1302 0784 E40D XRI 0D ; CHECK FOR CR
1303 0786 9850 JZ $CR
1304 0788 40 LDE
1305 0789 E45F XRI '0'+010 ; CHECK FOR SHIFT/0
1306 078B 9841 JZ $RUB ; CHECK FOR CTRL/H
1307 078D 40 LDE
1308 078E E408 XRI 8 ; CHECK FOR CTRL/U
1309 0790 9836 JZ $XH
1310 0792 40 LDE
1311 0793 E415 XRI 015 ; CHECK FOR CTRL/U
1312 0795 980F JZ $XU
1313 0797 40 LDE
1314 0798 E403 XRI 3 ; CHECK FOR CTRL/C

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1315 079A 9C1A      JNZ      $ENTER
1316 079C C45E      LDI      P3
1317 079E 3F        XPPC      P3
1318 079F C443      LDI      P3
1319 07A1 3F        XPPC      P3
1320 07A2 C40E      LDI      14
1321 07A4 90A9      JMP      E9
1322 07A6 C45E      *XU:    LDI      P3
1323 07A8 3F        XPPC      P3
1324 07A9 C455      LDI      P3
1325 07AB 3F        XPPC      P3
1326 07AC C40D      LDI      0D
1327 07AE 3F        XPPC      P3
1328 07AF C40A      LDI      0A
1329 07B1 3F        XPPC      P3
1330 07B2 909F      *2:    JMP      GETL
1331 07B4 909B      X15:   JMP      X14
1332 07B6 40        *ENTER: LDE
1333 07B7 C0D1      ST      01(P1)
1334 07B9 AAE7      ILD      CHNUM(P2)
1335 07BB E448      XRI      72
1336 07BD 9CB3      JNZ      $1
1337 07BF C40D      LDI      0D
1338 07C1 01        XAE
1339 07C2 40        LDE
1340 07C3 3F        XPPC      P3
1341 07C4 9012      JMP      $CR
1342 07C6 9087      E10:   JMP
1343 07C8 C420      *XH:   LDI      P3
1344 07CA 3F        XPPC      P3
1345 07CB C408      LDI      8
1346 07CD 3F        XPPC      P3
1347 07CE C2E7      *RUB:  LD      CHNUM(P2)
1348 07D0 98A0      JZ      $1
1349 07D2 BAE7      DLD      CHNUM(P2)
1350 07D4 C5FF      LD      0-1(P1)
1351 07D6 909A      JMP
1352 07D8 40        LDE
1353 07D9 C0D1      *CR:   ST      01(P1)
1354 07DB C40A      LDI      0A
1355 07DD 3F        XPPC      P3
1356 07DE C410      LDI      H(LBUF)
1357 07E0 35        XPAH      P1
1358 07E1 C4D6      LDI      L(LBUF)
1359 07E3 31        XPAL      P1
1360 07E4 90CE      X16:   JMP      X15
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370 07E6 C410      EVAL:  LDI      H(AESTK)
1371 07E8 37        XPAH      P3
1372 07EA C2FD      LD      LSTK(P2)
1373 07EC C3FF      XPAL      P3
1374 07EE 35        LD      -1(P3)
1375 07EF 01        XPAH      P1
1376 07F0 C3FE      XAE
1377 07F2 31        LD      -2(P3)
1378 07F3 CAEF      XPAL      P1
1379 07F5 C100      ST      0(P1)
1380 07F7 CBFE      LD      -2(P3)
1381 07F9 C400      LDI      0
1382 07FB CBFF      ST      -1(P3)
1383 07FD C2EF      LD      L0(P2)
1384 07FF 31        XPAL      P1
1385 0800 40        LDE
1386 0801 35        XPAH      P1
1387 0802 90B0      JMP      X15
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1397 0804 C410      MOVE:  LDI      H(AESTK)
1398 0806 37        XPAH      P3
1399 0807 C2FD      LD      LSTK(P2)
1400 0809 33        XPAL      P3
1401 080A C7FE      LD      0-2(P3)
1402 080C 01        XAE
1403 080D C7FF      LD      0-1(P3)
1404 080F CAEA      ST      TEMP(P2)
1405 0811 C7FF      LD      0-1(P3)
1406 0813 33        XPAL      P3
1407 0814 CAFD      LD      LSTK(P2)
1408 0816 C2EA      LD      TEMP(P2)
1409 0818 37        XPAH      P3
1410 0819 40        LDE
1411 081A CB00      ST      0(P3)
1412 081C 90C6      X17:   JMP      X16
1413 081E 90A6      E11:   JMP      E10
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1432 0820 C410      INSRT: LDI      H(AESTK)
1433 0822 37        XPAH      P3
1434 0823 C2FD      LD      LSTK(P2)
1435 0825 33        XPAL      P3
1436 0826 C301      LD      1(P3)
1437 0828 CAF7      ST      HILINE(P2)
1438 082A C300      LD      0(P3)
1439 082C CAF8      ST      L0LINE(P2)
1440 082E C2F1      LD      PILOW(P2)
1441 0830 33        XPAL      P3
1442 0831 C2F0      LD      PIHIGH(P2)
1443 0833 37        XPAH      P3
1444 0834 C404      LDI      4
1445 0836 CAE7      ST      CHNUM(P2)
1446 0838 C761      *1:    LD      01(P3)
1447 083A E40D      XRI      0D
1448 083C 9804      JZ
1449 083E AAE7      LLD
1450 0840 90F6      JMP
1451 0842 C2E7      *2:    LD
1452 0844 E404      XRI      4
1453 0846 9C02      JNZ
1454 0848 CAE7      ST
1455 084A C2E7      *3:    LD
1456 084C 01        XAE
1457 084D C2F2      LD
1458 084F 9406      ANI
1459 0851 047F      ST
1460 0853 CAF2      LABLHI(P2)
1461 0855 9018      JMP
1462 0857 C503      *4:    LD
1463 0859 40        LDE
1464 085A 02        CCL
1465 085B F4FC      ADI      -4
1466 085D 01        XAE
1467 085E C501      LD
1468 0860 E40D      *5:    XRI      0D
1469 0862 980B      JZ
1470 0864 40        LDE
1471 0865 02        CCL
1472 0866 F4FF      ADI      -1
1473 0868 01        XAE
1474 0869 90F3      JMP
1475 086B 90AF      *19:   JMP
1476 086D 90AF      E12:   JMP
1477 086F 40        *MOVE: LDE
1478 0870 DAE7      OR
1479 0872 98F7      JZ
1480 0874 C47A      LDI
1481 0876 CAFF      ST
1482 0878 C46A      LDI
1483 087A CAFC      ST
1484 087C C48A      LDI
1485 087E CAFE      ST
1486 0880 40        LDE
1487 0881 9860      JZ
1488 0883 9410      *DOWN: JP
1489 0885 C100      LD
1490 0887 C980      ST
1491 0889 C501      LD
1492 088B 94F8      JP
1493 088D C100      LD
1494 088F 94F4      JP
1495 0891 C980      ST
1496 0893 904E      *ADD:  JMP
1497 0895 C1FE      LD
1498 0897 CAEA      ST
1499 0899 C4FF      LDI
1500 089B C9FE      ST
1501 089D C450      LDI
1502 089F C9FF      ST
1503 08A1 C501      *UP1:  LD
1504 08A3 94F4      JP
1505 08A5 C100      LD
1506 08A7 94F8      JP
1507 08A9 35        XPAH      P1
1508 08AA CAEE      ST
1509 08AC 35        XPAH      P1
1510 08AD 31        XPAL      P1
1511 08AE CAEF      ST
1512 08B0 31        XPAL      P1
1513 08B1 C2EF      LD
1514 08B3 02        CCL
1515 08B4 70        ADE
1516 08B5 C400      LDI      0
1517 08B7 F2EE      ADD      HI(P2)
1518 08B9 E2EE      XOR      HI(P2)
1519 08BB D4F0      ANI      0F0
1520 08BD 9803      JZ
1521 08BF C400      LDI      0
1522 08C1 01        XAE
1523 08C2 C4F0      *UP2:  LDI
1524 08C4 C980      *UP3:  ST
1525 08C6 C5FF      LD
1526 08C8 94FA      JP
1527 08CA C101      LD
1528 08CC E450      XRI      80
1529 08CE 9804      JZ
1530 08D0 C100      LD
1531 08D2 90F0      JMP
1532 08D4 C2EA      *UP4:  LD
1533 08D6 C900      ST
1534 08D8 C40D      LD
1535 08DA C901      ST
1536 08DC 40        LDE
1537 08DD 9C04      JNZ
1538 08DF C402      LDI      2
1539 08E1 908A      E12A:  JMP
1540 08E3 C2E7      *ADD:  LD
1541 08E5 9884      JZ
1542 08E7 C2F1      X19A:  LD
1543 08E9 31        XPAL      P1
1544 08EA C2F0      LD
1545 08EC 35        XPAH      P1
1546 08ED C2F3      LD
1547 08EF 33        XPAL      P3
1548 08F0 C2F2      LD
1549 08F2 37        XPAH      P3
1550 08F3 C2F7      LD
1551 08F5 CF01      ST
1552 08F7 C2F8      LD
1553 08F9 CF01      ST
1554 08FB C2E7      LD
1555 08FD CF01      ST
1556 08FF C501      *ADD1: LD
1557 0901 CF01      ST
1558 0903 CF01      XRI      0D
1559 0905 9CF8      JNZ
1560 0907 90DC      JMP
1561 0909 C400      X20:   JS
1562 0910 90CF      E13:   JS
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1569 0912 BAFD      POPAE: DLD
1570 0914 BAFD      DLD
1571 0916 33        XPAL      P3
1572 0917 C410      LD
1573 0919 37        XPAH      P3
1574 091A C300      LD
1575 091C CAEF      ST
1576 091E C301      LD
1577 0920 CAEE      ST
1578 0922 90E5      HI(P2)
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1581 ;*****
1582 ;*          UNTIL          *
1583 ;*****
1584
1585 ; LOCAL
1586 0924 C2FF UNTIL: LD DOPTR(P2) ;CHECK FOR DO-STACK UNDERFLOW
1587 0926 01 XAE
1588 0927 40 LDE
1589 0928 E47A XRI L(DOSTAK)
1590 092A 9C04 JNZ $1
1591 092C C40F LDI 15
1592 092E 90E0 JMP E13
1593 0930 C2EF $1: LD L0(P2) ;CHECK FOR EXPRESSION = 0
1594 0932 DAEE OR HI(P2)
1595 0934 9806 JZ $REDO ;IF ZERO, REPEAT DO-LOOP
1596 0936 BAFF DLD DOPTR(P2) ;ELSE POP SAVE STACK
1597 0938 BAFF DLD DOPTR(P2)
1598 093A 90CD JMP X20 ;CONTINUE TO NEXT STMT
1599 093C 40 LDE ;POINT P3 AT DO-STACK
1600 093D 33 XPAL P3
1601 093E C410 LDI H(DOSTAK)
1602 0940 37 XPAH P3
1603 0941 C3FF LD -1(P3) ;LOAD P1 FROM DO STACK
1604 0943 35 XPAH P1
1605 0944 C3FE LD -2(P3)
1606 0946 31 XPAL P1 ;CURSOR NOW POINTS TO FIRST
1607 0947 90C0 JMP X20 ; STATEMENT OF DO-LOOP
1608
1609 ;*****
1610 ;*          STORE INTO STATUS REGISTER          *
1611 ;*****
1612
1613 ; THIS ROUTINE IMPLEMENTS THE STATEMENT:
1614 ; 'STAT' 'n' REL-EXP
1615
1616 1617 0949 C2EF MOVES: LD L0(P2) ;LOW BYTE GOES TO STATUS
1618 094B D4F7 ANI 0F7 ; BUT WITH IEN BIT CLEARED
1619 094D 07 CAS
1620 094E 90B9 X21: JMP X20
1621 0950 90BE E14: JMP E13
1622
1623 ;*****
1624 ;*          STAT FUNCTION          *
1625 ;*****
1626
1627 1628 0952 C410 STATUS: LDI H(AESTK)
1629 0954 37 XPAH P3 ;POINT P3 AT AE STACK
1630 0955 AAFD ILD LSTK(P2)
1631 0957 AAFD ILD LSTK(P2)
1632 0959 33 XPAL P3
1633 095A 06 CSA
1634 095B CBFE ST -2(P3) ;STATUS REG IS LOW BYTE
1635 095D C400 LDI 0
1636 095F CBFF ST -1(P3) ;ZERO IS HIGH BYTE
1637 0961 90EB JMP X21
1638
1639 ;*****
1640 ;*          MACHINE LANGUAGE SUBROUTINE          *
1641 ;*****
1642
1643 ; THIS ROUTINE IMPLEMENTS THE 'LINK' STATEMENT
1644
1645 1646 0963 C2EE CALLML: LD HI(P2) ;GET HIGH BYTE OF ADDRESS
1647 0965 37 XPAH P3
1648 0966 C2EF LD L0(P2) ;GET LOW BYTE
1649 0968 33 XPAL P3 ;P3 -> USER'S ROUTINE
1650 0969 C7FF LD 0-1(P3) ;CORRECT P3
1651 096B 3F XPPC ;CALL ROUTINE (PRAY IT WORKS)
1652 096C LDP P2,VARS ;RESTORE RAM POINTER
1653 0972 90DA JMP X21 ;RETURN
1654
1655 ;*****
1656 ;*          SAVE DO LOOP ADDRESS          *
1657 ;*****
1658
1659 ; THIS ROUTINE IMPLEMENTS THE 'DO' STATEMENT.
1660
1661 ; LOCAL
1662 1663 0974 C2FF SAVEDO: LD DOPTR(P2) ;CHECK FOR STACK OVERFLOW
1664 0976 E48A XRI L(FORSTK)
1665 0978 9C04 JNZ $1
1666 097A C40A LDI 10
1667 097C 90D2 JMP E14
1668 097E AAFD $1: ILD DOPTR(P2)
1669 0980 AAFD ILD DOPTR(P2)
1670 0982 33 XPAL P3
1671 0983 C410 LDI H(DOSTAK)
1672 0985 37 XPAH P3 ;P3 -> TOP OF DO STACK
1673 0986 35 XPAH P1 ;SAVE CURSOR ON THE STACK
1674 0987 CBFF ST -1(P3)
1675 0989 35 XPAH P1
1676 098A 31 XPAL P1
1677 098B CBFE ST -2(P3)
1678 098D 31 XPAL P1
1679 098E 90BE X22: JMP X21
1680
1681 ;*****
1682 ;*          TOP OF RAM FUNCTION          *
1683 ;*****
1684
1685 ; LOCAL
1686 1687 0990 C2E9 TOP: LD TEMP2(P2) ;SET P3 TO POINT TO
1688 0992 37 XPAH P3 ; START OF NIBL TEXT
1689 0993 C2E8 LD TEMP3(P2)
1690 0995 33 XPAL P3
1691 0996 C300 $0: LD (P3) ;HAVE WE HIT END OF TEXT?
1692 0998 9402 JP $1 ;NO - SKIP TO NEXT LINE
1693 099A 9007 JMP $2 ;YES - PUT CURSOR ON STACK
1694 099C C302 $1: LD 2(P3) ;GET LENGTH OF LINE
1695 099E 01 XAE
1696 099F C780 LD BEREGR(P3) ;SKIP TO NEXT LINE
1697 09A1 90F3 JMP $0 ;GO CHECK FOR EOF
1698 09A3 C702 $2: LD 02(P3) ;P3 := P3 + 2
1699 09A5 AAFD ILD LSTK(P2) ;SET P3 TO STACK, SAVING
1700 09A7 AAFD ILD LSTK(P2) ; OLD P3 (WHICH CONTAINS TOP)
1701 09A9 33 XPAL P3 ; ON IT SOMEHOW
1702 09AA 01 XAE
1703 09AB C410 LDI H(AESTK)
1704 09AD 37 XPAH P3
1705 09AE CBFF ST -1(P3)
1706 09B0 40 LDE
1707 09B1 CBFE ST -2(P3)
1708 09B3 90D9 JMP X22
1709
1710 ;*****
1711 ;*          SKIP TO NEXT NIBL LINE          *
1712 ;*****
1713
1714

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1715 09B5 C501 IGNORE: LD 01(P1) ;SCAN TIL WE'RE PAST
1716 09B7 E40D XRI 0D ; CARRIAGE RETURN
1717 09B9 9CFA JNZ IGNORE
1718 09BB 3F XPPC P3 ;YES - RETURN
1719
1720 ;*****
1721 ;*          MODULO FUNCTION          *
1722 ;*****
1723
1724 1725 09BC C2FD MODULO: LD LSTK(P2) ;THIS ROUTINE MUST BE
1726 09BE 33 XPAL P3 ; IMMEDIATELY AFTER A
1727 09BF C410 LDI H(AESTK) ; DIVIDE TO WORK CORRECTLY
1728 09C1 37 XPAH P3
1729 09C2 C303 LD 3(P3) ;GET LOW BYTE OF REMAINDER
1730 09C4 CBFE ST -2(P3) ;PUT ON STACK
1731 09C6 C302 LD 2(P3) ;GET HIGH BYTE OF REMAINDER
1732 09C8 CBFF ST -1(P3) ;PUT ON STACK
1733 09CA 90C2 X23: JMP X22
1734 09CC 90AE E16: JMP E15
1735
1736 ;*****
1737 ;*          RANDOM FUNCTION          *
1738 ;*****
1739
1740 ; LOCAL
1741 1742 09CE C408 RANDOM: LDI 8 ;LOOP COUNTER FOR MULTIPLY
1743 09D0 CAEB ST NUM(P2)
1744 09D2 C2E5 LD RNDX(P2)
1745 09D4 01 XAE
1746 09D5 C2E4 LD RNDY(P2)
1747 09D7 CAE9 ST TEMP2(P2)
1748 09D9 C2E5 $LOOP: LD RNDX(P2) ;MULTIPLY THE SEEDS BY 9
1749 09DB 02 CCL
1750 09DC 70 ADE
1751 09DD 01 XAE
1752 09DE C2E4 LD RNDY(P2)
1753 09E0 02 CCL
1754 09E1 F2E9 ADD TEMP2(P2)
1755 09E3 CAE4 ST RNDY(P2)
1756 09E5 BAEB DLD NUM(P2)
1757 09E7 9CF0 JNZ $LOOP
1758 09E9 40 LDE ;ADD 7 TO SEEDS
1759 09EA 02 CCL
1760 09EB F407 ADI 7
1761 09ED 01 XAE
1762 09EE C2E4 LD RNDY(P2)
1763 09F0 02 CCL
1764 09F1 F407 ADI 7
1765 09F3 1E RR
1766 09F4 CAE4 ST RNDY(P2)
1767 09F6 AE6 ILD RNDY(P2)
1768 09F8 9803 JZ $1 ;HAVE WE GONE THROUGH
1769 09FA 40 LDE ; 256 GENERATIONS?
1770 09FB CAE5 ST RNDX(P2) ;IF SO, SKIP GENERATING
1771 09FD C2FD $1: LD LSTK(P2) ;THE NEW RNDX
1772 09FF 33 XPAL P3 ;START MESSING WITH THE STACK
1773 0A00 C410 LDI H(AESTK)
1774 0A02 37 XPAH P3
1775 0A03 C401 LDI 1 ;FIRST PUT 1 ON STACK
1776 0A05 C800 ST (P3)
1777 0A07 C400 LDI 0
1778 0A09 CB01 ST 1(P3)
1779 0A0B C3FE LD -2(P3) ;PUT EXPR2 ON STACK
1780 0A0D CB02 ST 2(P3)
1781 0A0F C3FF LD -1(P3)
1782 0A11 CB03 ST 3(P3)
1783 0A13 C3FC LD -4(P3) ;PUT EXPR1 ON STACK
1784 0A15 CB04 ST 4(P3)
1785 0A17 C3FD LD -3(P3)
1786 0A19 CB05 ST 5(P3)
1787 0A1B C2E4 LD RNDY(P2) ;PUT RANDOM # ON STACK
1788 0A1D CBFE ST -2(P3)
1789 0A1F C2E5 LD RNDX(P2)
1790 0A21 E4FF XRI OFF
1791 0A23 D47F ANI 07F
1792 0A25 CBFF ST -1(P3)
1793 0A27 C706 LD 06(P3) ;ADD 6 TO STACK POINTER
1794 0A29 33 XPAL P3
1795 0A2A CAFD ST LSTK(P2)
1796 0A2C 909C X24: JMP X23
1797 0A2E 909C E16A: JMP E16
1798
1799 ;*****
1800 ;*          PUSH 1 ON ARITHMETIC STACK          *
1801 ;*****
1802
1803 1804 0A30 AAFD LIT1: ILD LSTK(P2)
1805 0A32 AAFD ILD LSTK(P2)
1806 0A34 33 XPAL P3
1807 0A35 C410 LDI H(AESTK)
1808 0A37 37 XPAH P3
1809 0A38 C400 LD 0
1810 0A3A CBFF ST -1(P3)
1811 0A3C C401 LDI 1
1812 0A3E CBFE ST -2(P3)
1813 0A40 90EA JMP X24
1814
1815 ;*****
1816 ;*          FOR-LOOP INITIALIZATION          *
1817 ;*****
1818
1819 ; LOCAL
1820 1821 0A42 C2FE SAVFOR: LD FORPTR(P2) ;CHECK FOR FOR STACK
1822 0A44 E4A6 XRI L(PCSTAK) ; OVERFLOW
1823 0A46 9C04 JNZ $1
1824 0A48 C40A LDI 10
1825 0A4A 90E2 E17: JMP E16A
1826 0A4C E4A6 $1: XRI L(PCSTAK)
1827 0A4E 31 XPAL P1 ;POINT P1 AT FOR STACK
1828 0A4F CAF1 ST PILOW(P2) ; SAVING OLD P1
1829 0A51 C410 LDI H(FORSTK)
1830 0A53 35 XPAH P1
1831 0A54 CAF0 ST PIHIGH(P2)
1832 0A56 C2FD LD LSTK(P2) ;POINT P3 AT AE STACK
1833 0A58 33 XPAL P3
1834 0A59 C410 LDI H(AESTK)
1835 0A5B 37 XPAH P3
1836 0A5C C3F9 LD -7(P3) ;GET VARIABLE INDEX
1837 0A5E CD01 ST 01(P1) ;SAVE ON FOR-STACK
1838 0A60 C3FC LD -4(P3) ;GET L(LIMIT)
1839 0A62 CD01 ST 01(P1) ;SAVE
1840 0A64 C3FD LD -3(P3) ;GET H(LIMIT)
1841 0A66 CD01 ST 01(P1) ;SAVE
1842 0A68 C3FE LD -2(P3) ;GET L(STEP)
1843 0A6A CD01 ST 01(P1) ;SAVE
1844 0A6C C3FF LD -1(P3) ;GET H(STEP)
1845 0A6E CD01 ST 01(P1) ;SAVE
1846 0A70 C2F1 LD PILOW(P2) ;GET L(P1)
1847 0A72 CD01 ST 01(P1) ;SAVE
1848 0A74 C2F0 LD PIHIGH(P2) ;GET H(P1)

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1849 0A76 CD01      ST      @1(P1)      ;SAVE
1850 0A78 35        XPAH   P1          ;RESTORE OLD P1
1851 0A79 C2F1      LD      P1LOW(P2)
1852 0A7B 31        XPAL   P1
1853 0A7C CAFE      ST      FORPTR(P2) ;UPDATE FOR STACK PTR
1854 0A7E C7FC      LD      @-4(P3)
1855 0A80 33        XPAL   P3
1856 0A81 CAFD      ST      LSTK(P2)   ;UPDATE AE STACK PTR
1857 0A83 90A7      X25:    JMP      X24
1858
1859
1860 ; *****
1861 ; * FIRST PART OF 'NEXT VAR' *
1862 ; *****
1863
1864 .LOCAL
1865 0A85 C2FE NEXTTV: LD      FORPTR(P2) ;POINT P1 AT FOR STACK,
1866 0A87 E48A      XRI      L(FORSTK) ;CHECKING FOR UNDERFLOW
1867 0A89 9C04      JNZ      $1
1868 0A8B C40B      LD      LDI
1869 0A8D 90B8      JMP      E17 ;REPORT ERROR
1870 0A8F E48A      $1:     XRI      L(FORSTK)
1871 0A91 31        XPAL   P1
1872 0A92 CAF1      ST      P1LOW(P2) ;SAVE OLD P1
1873 0A94 C410      LD      H(FORSTK)
1874 0A96 35        XPAH   P1
1875 0A97 CAF0      ST      PIHIGH(P2)
1876 0A99 C2FD      LD      LSTK(P2) ;POINT P3 AT AE STACK
1877 0A9B 33        XPAL   P3
1878 0A9C C410      LD      H(AESTK)
1879 0A9E 37        XPAH   P3
1880 0A9F C7FF      LD      @-1(P3) ;GET VARIABLE INDEX
1881 0AA1 E1F9      XOR      -7(P1) ;COMPARE WITH INDEX
1882 0AA3 9804      JZ       $10 ;ON FOR STACK: ERROR
1883 0AA5 C40C      LD      12 ;IF NOT EQUAL
1884 0AA7 90A1      E18:    JMP      E17
1885 0AA9 E1F9      $10:    XOR      -7(P1) ;RESTORE INDEX
1886 0AAB 01        XAE      ;SAVE IN EREG
1887 0AAC C2B0      LD      EREG(P2) ;GET L(VARIABLE)
1888 0AAE 02        CCL
1889 0AAF F1FC      ADD      -4(P1) ;ADD L(STEP)
1890 0AB1 C4B0      ST      EREG(P2) ;STORE IN VARIABLE
1891 0AB3 CB00      ST      (P3) ;AND ON STACK
1892 0AB5 C601      LD      @1(P2) ;INCREMENT RAM PTR
1893 0AB7 C2B0      LD      EREG(P2) ;GET H(VARIABLE)
1894 0AB9 F1FD      ADD      -3(P1) ;ADD H(STEP)
1895 0ABB C4B0      ST      EREG(P2) ;STORE IN VARIABLE
1896 0ABD CB01      LD      1(P3) ;AND ON STACK
1897 0ABF C6FF      ST      @-1(P2) ;RESTORE RAM POINTER
1898 0AC1 C1FA      LD      -6(P1) ;GET L(LIMIT)
1899 0AC3 CB02      ST      2(P3) ;PUT ON STACK
1900 0AC5 C1FB      LD      -5(P1) ;GET H(LIMIT)
1901 0AC7 CB03      ST      3(P3) ;PUT ON STACK
1902 0AC9 C1FD      LD      -3(P1) ;GET H(STEP)
1903 0ACB 9410      JP      $2 ;IF NEGATIVE, INVERT
1904 0ACD C404      LD      4 ;ITEMS ON A.E. STACK
1905 0ACE CAEB      ST      NUM(P2) ;NUM = LOOP COUNTER
1906 0AD1 C701      $LOOP: LD      @1(P3) ;GET BYTE FROM STACK
1907 0AD3 E4FF      XRI      OFF ;INVERT IT
1908 0AD5 CBFF      ST      -1(P3) ;PUT BACK ON STACK
1909 0AD7 BAEB      DLD      NUM(P2) ;DO UNTIL NUM = 0
1910 0AD9 9CF6      JNZ      $LOOP
1911 0ADB 9002      LD      $2:    LD      $3
1912 0ADD C704      $3:    LD      @4(P3) ;UPDATE AE STACK POINTER
1913 0ADF 33        XPAL   P3
1914 0AE0 CAFD      ST      LSTK(P2)
1915 0AE2 C2F1      LD      P1LOW(P2) ;RESTORE OLD P1
1916 0AE4 31        XPAL   P1
1917 0AE5 C2F0      LD      PIHIGH(P2)
1918 0AE7 35        XPAH   P1
1919 0AE8 9099      X26:    JMP      X25
1920
1921 ; *****
1922 ; * SECOND PART OF 'NEXT VAR' *
1923 ; *****
1924
1925 NEXTTV1: LD      LO(P2) ;IS FOR-LOOP OVER WITH?
1926 0AEA C2EF      JZ       $REDO ;NO - REPEAT LOOP
1927 0AEC 9808      LD      FORPTR(P2) ;YES - POP FOR-STACK
1928 0AEE C2FE      CCL
1929 0AF0 02        ADI      -7
1930 0AF1 F4F9      ST      FORPTR(P2)
1931 0AF3 CAFE      LD      P3 ;RETURN TO I.L. INTERPRETER
1932 0AF5 3F        $REDO: LD      FORPTR(P2) ;POINT P3 AT FOR STACK
1933 0AF6 C2FE      XPAL   P3
1934 0AF8 33        LD      H(FORSTK)
1935 0AF9 C410      XPAH   P3
1936 0AFB 37        LD      -1(P3) ;GET OLD P1 OFF STACK
1937 0AFC C3FF      LD      XPAH   P1
1938 0AFE 35        XPAL   P1
1939 0AFF C3FE      LD      -2(P3)
1940 0B01 31        XPAL   P1
1941 0B02 90E4      JMP      X26
1942 0B04 90A1      E19:    JMP      E18
1943
1944 ; *****
1945 ; * PRINT MEMORY AS STRING *
1946 ; *****
1947
1948 ; THIS ROUTINE IMPLEMENTS THE STATEMENT:
1949 ; 'PRINT' '$' FACTOR
1950
1951 .LOCAL
1952 0B06 C2EE PSTRNG: LD      HI(P2) ;POINT P1 AT STRING TO PRINT
1953 0B08 35        XPAH   P1
1954 0B09 C2EF      LD      LO(P2)
1955 0B0B 31        XPAL   P1
1956 0B0D C2F1      LD      P3,PUTC-1 ;POINT P3 AT PUTC ROUTINE
1957 0B0F C2F1      LD      @1(P1) ;GET A CHARACTER
1958 0B12 C501      $1:     XRI      OD ;IS IT A CARRIAGE RETURN?
1959 0B14 E4D0      JZ       X26 ;YES - WE'RE DONE
1960 0B16 98D0      XRI      OD ;NO - PRINT THE CHARACTER
1961 0B18 E4D0      XPCC   P3
1962 0B1A 3F        CSA      020 ;MAKE SURE NO ONE IS
1963 0B1B 06        ANI      $1 ;TYPING ON THE TTY
1964 0B1C D420      JNZ      X26 ;BEFORE REPEATING LOOP
1965 0B1E 9CF2      JMP      X26
1966 0B20 90C6
1967
1968 ; *****
1969 ; * INPUT A STRING *
1970 ; *****
1971
1972 ; THIS ROUTINE IMPLEMENTS THE STATEMENT:
1973 ; 'INPUT' '$' FACTOR
1974
1975 .LOCAL
1976 0B22 C2EE ISTRNG: LD      HI(P2) ;GET ADDRESS TO STORE THE
1977 0B24 37        XPAH   P3 ;STRING, PUT IT INTO P3
1978 0B25 C2EF      LD      LO(P2)
1979 0B27 33        XPAL   P3
1980 0B28 C501      $2:     LD      @1(P1) ;GET A BYTE FROM LINE BUFFER
1981 0B2A CF01      ST      @1(P3) ;PUT IT IN SPECIFIED LOCATION
1982 0B2C E4D0      XRI      OD
1983 0B2E 9CF8      JNZ      X26
1984 0B30 90B6      X27:    JMP      X26
1985
1986 ; *****
1987 ; * STRING CONSTANT ASSIGNMENT *
1988 ; *****
1989
1990 ; THIS ROUTINE IMPLEMENTS THE STATEMENT:
1991 ; '$' FACTOR '=' STRING
1992
1993 .LOCAL
1994 0B32 C2EF PUTSTR: LD      LO(P2) ;GET ADDRESS TO STORE STRING,
1995 0B34 33        XPAH   P3 ;PUT IT INTO P3
1996 0B36 C2EE      LD      HI(P2)
1997 0B38 37        XPAH   P3
1998 0B3A C501      $LOOP: LD      @1(P1) ;GET A BYTE FROM STRING
1999 0B3C E422      XRI      -1 ;CHECK FOR END OF STRING
2000 0B3E 980E      JZ       $END ;SEND
2001 0B40 C2F1      LD      -1(P1) ;MAKE SURE THERE'S NO CR
2002 0B42 90C4      JNZ      $1
2003 0B44 C407      LD      7
2004 0B46 90BE      JMP      E19 ;ERROR IF CARRIAGE RETURN
2005 0B48 CF01      $1:     ST      @1(P3) ;RESTORE CHARACTER
2006 0B4A E4D0      XRI      OD ;PUT IN SPECIFIED LOCATION
2007 0B4C CF01      ST      @1(P3) ;GET NEXT CHARACTER
2008 0B4E 90EC      JMP      $LOOP ;APPEND CARRIAGE RETURN
2009 0B50 C4D0      LD      OD ;TO STRING
2010 0B52 CB00      ST      (P3)
2011 0B54 90DE      JMP      X27
2012
2013 ; *****
2014 ; * MOVE STRING *
2015 ; *****
2016
2017 ; THIS ROUTINE IMPLEMENTS THE STATEMENT:
2018 ; '$' FACTOR '=' '$' FACTOR
2019
2020 .LOCAL
2021 0B52 C2FD MOVSTR: LD      LSTK(P2) ;POINT P3 AT A.E. STACK
2022 0B54 33        XPAH   P3
2023 0B56 C410      LD      H(AESTK)
2024 0B58 C410      XPAH   P3
2025 0B5A C7FF      LD      @-1(P3) ;GET ADDRESS OF SOURCE STRING
2026 0B5C C7FF      LD      @-1(P3) ;INTO P1
2027 0B5E C7FF      LD      @-1(P3)
2028 0B60 31        XPAL   P1
2029 0B62 C7FF      LD      @-1(P3) ;GET ADDRESS OF DESTINATION
2030 0B64 01        XAE      @-1(P3) ;STRING INTO P3
2031 0B66 C7FF      LD      P3
2032 0B68 33        XPAL   P3
2033 0B6A C4FD      ST      LSTK(P2) ;UPDATE STACK POINTER
2034 0B6C 40        LDE
2035 0B6E 37        XPAH   P3
2036 0B70 C501      $LOOP: LD      @1(P1) ;GET A SOURCE CHARACTER
2037 0B72 CF01      ST      @1(P3) ;SEND IT TO DESTINATION
2038 0B74 CF01      XRI      OD ;REPEAT UNTIL CARRIAGE RET.
2039 0B76 98C0      JZ       X27
2040 0B78 06        CSA
2041 0B7A 06        ANI      020
2042 0B7C 9CF3      JNZ      $LOOP
2043 0B7E 90B9      JMP      X27
2044
2045 ; *****
2046 ; * PUT PAGE NUMBER ON STACK *
2047 ; *****
2048
2049 0B77 AAFD PUTPG: ILD      LSTK(P2)
2050 0B79 AAFD ILD      LSTK(P2)
2051 0B7B 33        XPAL   P3
2052 0B7D C410      LD      H(AESTK)
2053 0B7F 37        XPAH   P3
2054 0B81 C2F6      LD      PAGE(P2)
2055 0B83 CBFE      ST      -2(P3)
2056 0B85 C400      LD      0
2057 0B87 CBFF      ST      -1(P3)
2058 0B89 90A7      JMP      X27
2059
2060 ; *****
2061 ; * ASSIGN NEW PAGE *
2062 ; *****
2063
2064 .LOCAL
2065 0B89 C2FE NUPAGE: LD      LO(P2) ;GET PAGE # FROM STACK,
2066 0B8B D407      ANI      7 ;GET THE LOW 3 BITS
2067 0B8D 9C02      JNZ      $0 ;PAGE 0 BECOMES PAGE 1
2068 0B8F C401      LD      1
2069 0B91 CAF6      $0:     ST      PAGE(P2)
2070 0B93 3F        XPPC   P3 ;RETURN
2071
2072 ; *****
2073 ; * FIND START OF PAGE *
2074 ; *****
2075
2076 ; THIS ROUTINE COMPUTES THE START OF THE CURRENT TEXT PAGE,
2077 ; STORING THE ADDRESS IN TEMP2(P2) [THE HIGH BYTE], AND
2078 ; TEMP3(P2) [THE LOW BYTE].
2079
2080 0B94 C2F6 FNDPGE: LD      PAGE(P2)
2081 0B96 E401      XRI      1 ;SPECIAL CASE IS PAGE 1, BUT
2082 0B98 9C09      JNZ      $1 ;OTHERS ARE CONVENTIONAL
2083 0B9A C411      LD      H(PGM) ;PAGE 1 STARTS AT 'PGM'
2084 0B9C C4E9      ST      L(P2) ;L(P2)
2085 0B9E C420      LD      L(P1)
2086 0BA0 CAEB      ST      TEMP3(P2)
2087 0BA2 3F        XPPC   P3 ;RETURN
2088 0BA4 E401      $1:     XRI      1 ;RESTORE PAGE #
2089 0BA6 01        XAE      ;SAVE IT
2090 0BA8 C404      LD      4 ;LOOP COUNTER = 4
2091 0BAE C4E9      ST      NUM(P2) ;MULTIPLY PAGE# BY 16
2092 0BAC 02        $LOOP: LD      CCL
2093 0BAE 70        ADE
2094 0BAD 01        XAE
2095 0BAE BAEB      DLD      NUM(P2)
2096 0BB0 9CF8      JNZ      $LOOP
2097 0BB2 40        LDE
2098 0BB4 CAE9      ST      TEMP2(P2) ;TEMP2 HAS HIGH BYTE
2099 0BB6 C402      LD      2 ;OF ADDRESS NOW
2100 0BB8 C4E9      ST      TEMP3(P2) ;LOW BYTE IS ALWAYS 2
2101 0BB9 3F        XPPC   P3
2102
2103 ; *****
2104 ; * MOVE CURSOR TO NEW PAGE *
2105 ; *****
2106
2107 0BBA C2E9 CHPAGE: LD      TEMP2(P2) ;PUT START OF PAGE
2108 0BBB 35        XPAH   P1 ;INTO P1. THIS ROUTINE

```


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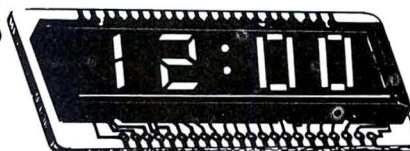
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7402-19c	7416-69c	7473-39c	7492-75c	74157-95c
74LS02-49c	7420-19c	7474-35c	7493-69c	74161-95c
7404-19c	7430-19c	7475-35c	7495-75c	74164-110
74LS04-49c	7432-34c	7476-35c	7496-89c	74165-110
7408-19c	7437-39c	7478-35c	74121-38c	74174-95c
74LS08-49c	7438-39c	7480-49c	74123-65c	74181-250
7406-29c	7440-19c	7483-95c	74132-170	74191-125
7408-19c	7447-85c	7485-95c	74S138-1.95	74192-125
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SOFTWARE SECTION

MICROCOMPUTER DEVELOPMENT SOFTWARE

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2115' 0BBD C2E8      LD      TEMP3(P2)      ; MUST BE CALLED RIGHT
2116 0BBF 31         XPAL    P1              ; AFTER 'FNDPGE'
2117 0BC0 3F         XPC     P3              ; RETURN
2118
2119
2120 ; *****
2121 ; *      DETERMINE CURRENT PAGE      *
2122 ; *****
2123
2124 0BC1' 35      DETPGE: XPAH    P1              ; CURRENT PAGE IS HIGH
2125 0BC2 01         XAE      -1              ; PART OF CURSOR DIVIDED
2126 0BC3 40         LDE      -1              ; BY 16
2127 0BC4 35      XPAH    P1
2128 0BC5 40         LDE
2129 0BC6 1C      SR
2130 0BC7 1C      SR
2131 0BC8 1C      SR
2132 0BC9 1C      SR
2133 0BCA CAF6     ST      PAGE(P2)
2134 0BCC 3F      XPC     P3              ; RETURN
2135
2136
2137 ; *****
2138 ; *      CLEAR CURRENT PAGE      *
2139 ; *****
2140
2141 0BCD C2E9     NEWPGM: LD      TEMP2(P2)      ; POINT P1 AT CURRENT PAGE
2142 0BCF 35      XPAH    P1
2143 0BD0 C2E8     LD      TEMP3(P2)
2144 0BD2 31      XPAL    P1
2145 0BD3 C40D     LDI      0D              ; PUT DUMMY END-OF-LINE
2146 0BD5 C9FF     ST      -1(P1)          ; JUST BEFORE TEXT
2147 0BD7 CAFF     LDI      -1              ; PUT -1 AT START OF TEXT
2148 0BD9 C900     ST      (P1)
2149 0BDB C901     ST      1(P1)
2150 0BD0 3F      XPC     P3              ; RETURN
2151
2152
2153 ; *****
2154 ; *      FIND LINE NUMBER IN TEXT  *
2155 ; *****
2156
2157 ; INPUTS: THE START OF THE CURRENT PAGE IN TEMP2 AND TEMP3,
2158 ;          THE LINE NUMBER TO LOOK FOR IN LO AND HI.
2159 ; OUTPUTS: THE ADDRESS OF THE FIRST LINE IN THE NIBL TEXT
2160 ;          WHOSE LINE NUMBER IS GREATER THAN OR EQUAL TO THE
2161 ;          NUMBER IN HI AND LO, RETURNED IN ADRL0 AND ADRL1
2162
2163 ; LOCAL
2164 0BDE C2E9     FNDLBL: LD      TEMP2(P2)      ; POINT P1 AT START OF TEXT
2165 0BE0 35      XPAH    P1
2166 0BE1 C2E8     LD      TEMP3(P2)
2167 0BE3 31      XPAL    P1
2168 0BE4 C100     #1: LD      (P1)              ; HAVE WE HIT END OF TEXT?
2169 0BE6 E4FF     XRI      OFF              ; YES - STOP LOOKING
2170 0BE8 9412     JP      $2              ; NO - COMPARE LINE NUMBERS
2171 0BEA 03      SCL      -1              ; BY SUBTRACTING
2172 0BED C101     LD      1(P1)
2173 0BED FAEF     CAD      LO(P2)
2174 0BEF C100     LD      0(P1)
2175 0BF1 FAEF     CAD      HI(P2)
2176 0BF3 9407     JP      $2              ; IS TEXT LINE # >= LINE #?
2177 0BF5 C102     LD      2(P1)          ; YES - STOP LOOKING
2178 0BF7 01      XAE      -1              ; NO - TRY NEXT LINE IN TEXT
2179 0BF8 C580     LD      @EREG(P1)        ; SKIP LENGTH OF LINE
2180 0BFA 90E8     JMP      $1
2181 0BFC 31      #2: XPAH    P1              ; SAVE ADDRESS OF FOUND LINE
2182 0BFD CAF3     ST      LABLLO(P2)        ; IN LABLHI AND LABLLO
2183 0BFF 31      XPAL    P1
2184 0C00 35      XPAH    P1
2185 0C01 CAF2     ST      LABLHI(P2)
2186 0C03 35      XPAH    P1
2187 0C04 C2EF     LD      LO(P2)          ; WAS THERE AN EXACT MATCH?
2188 0C06 E101     XOR      1(P1)
2189 0C08 9C07     JNZ      $3
2190 0C0A C2EE     LD      HI(P2)
2191 0C0C E100     XOR      0(P1)
2192 0C0E 9C01     JNZ      $3
2193 0C10 3F      JFPC    P3
2194 0C11 C2F2     #3: LD      LABLHI(P2)    ; SET SIGN BIT OF HIGH PART
2195 0C13 DC80     ORI      080            ; OF ADDRESS TO INDICATE
2196 0C15 CAF2     ST      LABLHI(P2)      ; INEXACT MATCH OF LINE #'S
2197 0C17 3F      XPC     P3
2198
2199 ; PAGE / I. L. MACROS /
2200
2201 ; *****
2202 ; *      I. L. MACROS      *
2203 ; *****
2204
2205 ; LOCAL
2206
2207 2000 #TSTBIT = TSTBIT*256
2208 8000 #CALBIT = CALBIT*256
2209 4000 #JMPBIT = JMPBIT*256
2210
2211 ; MACRO TST.FAIL,A,B
2212 .DBYTE #TSTBIT:FAIL
2213 .IF #=2
2214 .ASCII 'A':080
2215 .ELSE
2216 .ASCII 'B':080
2217 .BYT E
2218 .ENDIF
2219 .ENDM
2220
2221 ; MACRO TSTCR.FAIL
2222 .DBYTE #TSTBIT:FAIL
2223 .BYT E
2224 .ENDIF
2225 .ENDM
2226
2227 ; MACRO TSTV.FAIL
2228 .ADDR ISTVAR
2229 .DBYTE FAIL
2230 .ENDM
2231
2232 ; MACRO TSTN.FAIL
2233 .ADDR TSTNUM
2234 .DBYTE FAIL
2235 .ENDM
2236
2237 ; MACRO JUMP.ADR
2238 .DBYTE #JMPBIT:ADR
2239 .ENDM
2240
2241 ; MACRO CALL.ADR
2242 .DBYTE #CALBIT:ADR
2243 .ENDM
2244
2245 ; MACRO DO
2246 .MLOC I
2247 .SET I,1
2248 .DO #
2249 .ADDR #I

```

```

2249 .SET I,I+1
2250 .ENDDO
2251 .ENDM
2252 .PAGE / I. L. TABLE /
2253
2254 ; *****
2255 ; *      I. L. TABLE      *
2256 ; *****
2257
2258 0C18 START: DO NLINE
2259 0C1A PROMPT: DO OETL
2260 0C1C TSTCR PRMPT1
2261 0C1F JUMP PROMPT
2262 0C21 LIST PRMPT1: TSTN
2263 0C25 DO FNDPGE, XCHGP1, POPAE, FNDLBL, INSR
2264 0C2F JUMP PROMPT
2265
2266 0C31 LIST: TST RUN, 'LIS', 'T'
2267 0C37 DO FNDPGE
2268 0C39 TSTN LIST1
2269 0C3D DO POPAE, FNDLBL
2270 0C41 JUMP LIST2
2271 0C43 LIST1: DO CHPAGE
2272 0C45 LIST2: DO LST
2273 0C47 LIST3: CALL PRNUM
2274 0C49 DO LST3
2275 0C4B JUMP START
2276
2277 0C4D RUN: TST CLR, 'RU', 'N'
2278 0C52 DO DONE
2279 0C54 BEGIN: DO FNDPGE, CHPAGE, STRT, NXT
2280
2281 0C5C CLR: TST NEW, 'CLEA', 'R'
2282 0C63 DO DONE, CLEAR, NXT
2283
2284 0C69 NEW: TST STMT, 'NE', 'W'
2285 0C6E TSTN DFAULT
2286 0C72 JUMP NEW1
2287 0C74 DFAULT: DO LIT1
2288 0C76 NEW1: DO DONE, POPAE, NUPAGE, FNDPGE, NEWPGM, NXT
2289
2290 0C82 STMT: TST LET, 'LE', 'T'
2291 0C87 LET: TSTV AT
2292 0C8E TST SYNTAX, '='
2293 0C8E CALL RELEXP
2294 0C90 DO STORE, DONE, NXT
2295 0C96 AT: TST IF, 'B'
2296 0C99 CALL FACTOR
2297 0C9B TST SYNTAX, '='
2298 0C9E CALL RELEXP
2299 0CA0 DO MOVE, DONE, NXT
2300
2301 0CA6 IF: TST UNT, 'I', 'F'
2302 0CAA CALL RELEXP
2303 0CAC TST IF1, 'THE', 'N'
2304 0CB2 IF1: DO POPAE, CMFR
2305 0CB6 JUMP STMT
2306
2307 0CB8 UNT: TST DO, 'UNT', 'L'
2308 0CBF DO CKMODE
2309 0CC1 CALL RELEXP
2310 0CC3 DO DONE, POPAE, UNTIL, DETPGE, NXT
2311
2312 0CCD DO: TST GOTO, 'D', 'O'
2313 0CD1 DO CKMODE, DONE, SAVADO, NXT
2314
2315 0CD9 GOTO: TST RETURN, 'G', 'O'
2316 0CDB TST GOSUB, 'T', 'O'
2317 0CE1 CALL RELEXP
2318 0CE3 DO DONE
2319 0CE5 JUMP G01
2320 0CE7 GOSUB: TST SYNTAX, 'SU', 'B'
2321 0CEC CALL RELEXP
2322 0CEE DO DONE, SAV
2323 0CF2 G01: DO FNDPGE, POPAE, FNDLBL, XFER, NXT
2324
2325 0CFC RETURN: TST NEXT, 'RETUR', 'N'
2326 0D04 DO DONE, RSTR, DETPGE, NXT
2327
2328 0D0C NEXT: TST FOR, 'NEX', 'T'
2329 0D12 DO CKMODE
2330 0D14 TSTV SYNTAX
2331 0D18 DO DONE, NEXTV
2332 0D1C CALL GTROP
2333 0D1E DO POPAE, NEXTV1, DETPGE, NXT
2334
2335 0D26 FOR: TST STAT, 'FO', 'R'
2336 0D2B DO CKMODE
2337 0D2D TSTV SYNTAX
2338 0D31 TST SYNTAX, '='
2339 0D34 CALL RELEXP
2340 0D36 TST SYNTAX, 'T', 'O'
2341 0D3A CALL RELEXP
2342 0D3C TST FOR1, 'STE', 'P'
2343 0D42 CALL RELEXP
2344 0D44 JUMP FOR2
2345 0D46 FOR1: DO LIT1
2346 0D48 FOR2: DO DONE, SAVFOR, STORE, NXT
2347
2348 0D50 STAT: TST PGE, 'STA', 'T'
2349 0D56 TST SYNTAX, '='
2350 0D59 CALL RELEXP
2351 0D5B DO POPAE, MOVESR
2352 0D5F DO DONE, NXT
2353
2354 0D63 PGE: TST DOLLAR, 'PA', 'G'
2355 0D69 TST SYNTAX, '='
2356 0D6C CALL RELEXP
2357 0D6E DO DONE, POPAE, NUPAGE, FNDPGE, CHPAGE, NXT
2358
2359 0D7A DOLLAR: TST PRINT, '$'
2360 0D7D CALL FACTOR
2361 0D7F TST SYNTAX, '='
2362 0D82 TST DOLR1, '='
2363 0D85 DO POPAE, PUTSTR
2364 0D89 JUMP DOLR2
2365 0D8B DOLR1: TST SYNTAX, '$'
2366 0D8E CALL FACTOR
2367 0D90 DO XCHGP1, MOVSTR, XCHGP1
2368 0D96 DOLR2: DO DONE, NXT
2369
2370 0D9A PRINT: TST INPUT, 'P', 'R'
2371 0D9E TST PR1, 'IN', 'T'
2372 0DA3 PR1: TST PR2, 'N'
2373 0DA6 DO PRS
2374 0DA8 JUMP COMMA
2375 0DAA PR2: TST PR3, '$'
2376 0DAD CALL FACTOR
2377 0DAF DO XCHGP1, POPAE, PSTRNG, XCHGP1
2378 0DB7 JUMP COMMA
2379 0DB9 PR3: CALL RELEXP
2380 0DBB COMMA: TST PR4, 'N'
2381 0DBD PR4: TST PR1
2382 0DC0 JUMP

```


DIODES/ZENERS

1N914	100v	10mA	.05
1N4004	400v	1A	.08
1N4005	600v	1A	.08
1N4007	1000v	1A	.15
1N4148	75v	10mA	.03
1N753A	6.2v	z	.25
1N758A	10v	z	.25
1N759A	12v	z	.25
1N4733	5.1v	z	.25
1N5243	13v	z	.25
1N5244B	14v	z	.25
1N5245B	15v	z	.25

SOCKETS/BRIDGES

8-pin	pcb	.25	ww	.45
14-pin	pcb	.25	ww	.40
16-pin	pcb	.25	ww	.40
18-pin	pcb	.25	ww	.75
22-pin	pcb	.45	ww	.75
24-pin	pcb	.35	ww	1.25
28-pin	pcb	.35	ww	1.45
40-pin	pcb	.50	ww	1.95
Molex pins	.01	To-3 Sockets	.25	
2 Amp Bridge	100-prv		1.20	
25 Amp Bridge	200-prv		2.50	

TRANSISTORS, LEDS, etc.

2N2222	NPN			.10
2N2907	PNP			.15
2N3740	PNP	1A	60v	.25
2N3906	PNP			.10
2N3055	NPN	15A	60v	.50
LED	Green, Red, Clear			.15
D.L. 747	7 seg 5/8" high			1.95
XAN72	7 seg com-anode			1.50
FND 359	Red 7 seg com-cathode			1.00

C MOS

4000	.20
4001	.20
4002	.25
4004	4.95
4006	1.20
4007	.40
4008	1.20
4009	.25
4010	.45
4011	.20
4012	.25
4013	.40
4014	1.10
4015	.95
4016	.35
4017	1.10
4018	1.10
4019	.70
4020	.85
4021	1.35
4022	1.15
4023	.25
4024	.95
4025	.35
4026	1.95
4027	.50
4028	.95
4030	.45
4033	1.95
4034	2.45
4035	1.25
4040	1.35
4042	.95
4043	1.25
4044	.95
4046	1.50
4049	.80
4050	.70
4066	1.35
4069	.40
4071	.35
4082	.45

- T T L -

7400	.15	7474	.40	74193	.85	74S00	.55
7401	.15	7475	.45	74194	1.45	74S02	.55
7402	.20	7476	.20	74195	.95	74S03	.50
7403	.25	7480	.65	74196	1.50	74S10	.45
7404	.15	7483	1.00	74197	1.25	74S11	.45
7405	.25	7485	1.05	74198	2.35	74S20	.50
7406	.45	7486	.40	74367	.85	74S40	.30
7407	.55	7489	2.50			74S51	.45
7408	.25	7490	.40			74S64	.30
7409	.15	7491	1.15	75108A	.35	74S74	.50
7410	.15	7492	.95	75110	.35	74S112	1.50
7411	.25	7493	.45	75491	.50	74S133	.45
7412	.30	7494	1.25	75492	.50	74S140	.75
7413	.65	7495	.85			74S151A	.45
7414	1.10	7496	.95	74H00	.25	74S153	.45
7416	.25	74100	1.85	74H01	.25	74S158	.45
7417	.50	74107	.45	74H04	.25	74S194	1.50
7420	.15	74121	.40	74H05	.25	74S257 (8123)	.25
7426	.40	74122	.55	74H15	.30	74LS00	.45
7427	.45	74123	.55	74H20	.30	74LS01	.45
7430	.15	74125	.45	74H22	.40	74LS02	.45
7432	.45	74132	1.35	74H30	.25	74LS04	.55
7437	.45	74141	1.30	74H40	.25	74LS08	.45
7438	.35	74150	1.00	74H52	.15	74LS09	.45
7440	.25	74151	.95	74H53J	.25	74LS10	.45
7441	1.15	74153	.95	74H55	.25	74LS11	.45
7442	.65	74154	.75	74H72	.55	74LS20	.50
7443	.95	74156	1.15	74H101	.75	74LS21	.25
7444	.95	74157	.75	74H103	.75	74LS22	.25
7445	.95	74161	1.25	74H106	.95	74LS32	.55
7446	.95	74163	1.25			74LS37	.40
7447	.95	74164	.95			74LS40	.55
7448	1.20	74165	1.50			74LS42	1.75
7450	.25	74166	1.35			74LS52	1.45
7451	.25	74175	.95	74L00	.35	74LS74	.95
7453	.25	74176	1.25	74L02	.35	74LS90	1.30
7454	.25	74180	.85	74L03	.30	74LS93	1.00
7460	.40	74181	3.25	74L10	.35	74LS107	.95
7470	.45	74182	.95	74L30	.45	74LS153	1.20
7472	.45	74190	1.75	74L47	1.95	74LS157	.85
7473	.35	74192	1.65	74L75	.55	74LS164	1.90
						74LS368	.70

9000 SERIES

9301	1.00
9309	.45
9602	1.50

MEMORY, CLOCKS

74S188 (8223)	3.00
8080	26.50
MM1702A	10.50
MM5314	3.50
MM5316	3.95
2102-1	1.75
2102-L1	1.95
TR 1602A	6.95

LINEARS, REGULATORS, etc.

MCT2	.95	LM320K5	1.65	LM340T-24	1.25	LM723	.45
8038	3.95	LM320K12	1.65	LM340K-12	2.15	LM725	1.95
LM201AH	.75	LM320T12	1.65	LM340K-15	1.65	LM739	1.50
LM301AH	.25	LM320T15	1.65	LM340K-18	1.65	LM741 8-14	.25
LM308AH	1.00	LM339	1.65	LM340K-24	1.25	LM747	1.10
LM309H	.65	7805(340T-5)	1.00	LM373	1.95	LM1307	1.25
LM309K	.90	LM340T-12	1.25	LM380	.95	LM1458	.95
LM310	1.15	LM340T-15	1.25	LM709	.30	LM3900	.65
LM311	1.35	LM340T-18	1.65	LM711	.45	LM75451	.65
						NE555	.50
						NE556	1.10
						NE565	.95
						NE566	1.75
						NE567	1.35
						SN72720	.35
						SN72820	.35

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SOFTWARE SECTION

MICROCOMPUTER DEVELOPMENT SOFTWARE

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2383 ODC2 PR4: TST PR5, ' '
2384 ODC5 JUMP PR6
2385 ODC7 PR5: DO
2386 ODC9 PR6: DO DONE, NXT
2387
2388 ODCD INPUT: TST END, 'INPUT', 'T'
2389 ODD4 DO CKMODE
2390 ODD6 TSTV IN2
2391 ODDA DO XCHGP1, GETL
2392 ODD6 IN1: CALL RELEXP
2393 ODE0 DO STORE, XCHGP1
2394 ODE4 TST IN3, ' '
2395 ODE7 TSTV SYNTAX
2396 ODEB DO XCHGP1
2397 ODED TST SYNTAX, ' '
2398 ODF0 JUMP IN1
2399 ODF2 IN2: TST SYNTAX, ' '
2400 ODF5 CALL FACTOR
2401 ODF7 DO XCHGP1, GETL, POPAE, ISTRNG, XCHGP1
2402 OE01 IN3: DO DONE, NXT
2403
2404 OE05 END: TST ML, 'EN', 'D'
2405 OE0A DO DONE, BREAK
2406
2407 OE0E ML: TST REM, 'LIN', 'K'
2408 OE14 CALL RELEXP
2409 OE16 DO DONE, XCHGP1, POPAE, CALLML, XCHGP1, NXT
2410
2411 OE22 REM: TST SYNTAX, 'RE', 'M'
2412 OE27 DO IGNORE, NXT
2413
2414 OE2B SYNTAX: DO ERR
2415 OE2D ERRNUM: CALL PRNUM
2416 OE2F DO FIN
2417
2418 ; NOTE: EACH RELATIONAL OPERATOR (EQ, LEQ, ETC.) DOES AN
2419 ; AUTOMATIC 'RTN' (THIS SAVES VALUABE BYTES!)
2420
2421 OE31 RELEXP: CALL EXPR
2422 OE33 TST REL1, '='
2423 OE36 CALL EXPR
2424 OE38 DO EQ
2425 OE3A REL1: TST REL4, '<'
2426 OE3D TST REL2, '='
2427 OE40 CALL EXPR
2428 OE42 DO LEQ
2429 OE44 REL2: TST REL3, '>'
2430 OE47 CALL EXPR
2431 OE49 DO NEQ
2432 OE4B REL3: CALL EXPR
2433 OE4D DO LSS
2434 OE4F REL4: TST RETEXP, '>'
2435 OE52 TST REL5, '='
2436 OE55 CALL EXPR
2437 OE57 DO GEQ
2438 OE59 REL5: CALL EXPR
2439 OE5B GTROP: DO GTR
2440
2441 OE5D EXPR: TST EX1, ' '
2442 OE60 CALL TERM
2443 OE62 DO NEG
2444 OE64 JUMP EX3
2445 OE66 EX1: TST EX2, '+'
2446 OE69 EX2: CALL TERM
2447 OE6B EX3: TST EX4, '+'
2448 OE6E CALL TERM
2449 OE70 DO ADD
2450 OE72 JUMP EX3
2451 OE74 EX4: TST EX5, ' '
2452 OE77 CALL TERM
2453 OE79 DO SUB
2454 OE7B EX5: JUMP EX3
2455 OE7D EX5: TST RETEXP, 'O', 'R'
2456 OE81 CALL TERM
2457 OE83 DO OROP
2458 OE85 JUMP EX3
2459 OE87 RETEXP: DO RTN
2460
2461 OE89 TERM: CALL FACTOR
2462 OE8B T1: TST T2, '*'
2463 OE8E CALL FACTOR
2464 OE90 DO MUL
2465 OE92 JUMP T1
2466 OE94 T2: TST T3, '/'
2467 OE97 CALL FACTOR
2468 OE99 DO DIV
2469 OE9B JUMP T1
2470 OE9D T3: TST RETEXP, 'AN', 'D'
2471 OEA2 CALL FACTOR
2472 OEA4 DO ANDOP
2473 OEA6 JUMP T1
2474
2475 OEA8 FACTOR: TSTV F1
2476 OEAC DO IND, RTN
2477 OEBO F1: TSTN F2
2478 OEBA DO RTN
2479 OEBC F2: TST F3, '#'
2480 OEBC DO HEX, RTN
2481 OEBC F3: TST F4, '('
2482 OECC CALL RELEXP
2483 OECC TST SYNTAX, ')'
2484 OECC DO RTN
2485 OECC F4: TST F5, '@'
2486 OECC CALL FACTOR
2487 OECC DO EVAL, RTN
2488 OECC F5: TST F6, 'ND', 'T'
2489 OECC CALL FACTOR
2490 OECC DO NOTOP, RTN
2491 OECC F6: TST F7, 'STA', 'T'
2492 OECC DO STATUS, RTN
2493 OECC F7: TST F8, 'TO', 'P'
2494 OECC DO FNDPGE, TOP, RTN
2495 OECC F8: TST F9, 'MO', 'D'
2496 OECC DO DOUBLE
2497 OECC F9: DO DIV, MODULO, RTN
2498 OECC F9: TST F10, 'RN', 'D'
2499 OECC CALL DOUBLE
2500 OECC DO RANDOM, SUB, ADD, DIV, MODULO, ADD, RTN
2501 OECC F10: TST SYNTAX, 'PAG', 'E'
2502 OECC DO PUTPGE, RTN
2503
2504 OECC DOUBLE: TST SYNTAX, '{'
2505 OECC CALL RELEXP
2506 OECC F21: TST SYNTAX, ' '
2507 OECC F24: CALL RELEXP
2508 OECC F26: TST SYNTAX, '}'
2509 OECC F29: DO RTN
2510
2511 OF2B PRNUM: DO XCHGP1, PRN
2512 OF2F PRNUM1: DO DIV, PRN1, XCHGP1, RTN
2513
2514 PAGE 'ERROR MESSAGES'
2515
2516 ; *****
2517 ; * ERROR MESSAGES
2518 ; *****

```

```

2517 ; *****
2518
2519 ; MACRO MESSAGE, A, B
2520 ; ASCII 'A'
2521 ; BYTE 'B'!080
2522 ; ENDM
2523
2524 OF37 MESOS: MESSAGE 'ERRO', 'R' ; 1
2525 OF3D MESSAGE 'ARE', 'A' ; 2
2526 OF41 MESSAGE 'STM', 'T' ; 3
2527 OF45 MESSAGE 'CHA', 'R' ; 4
2528 OF49 MESSAGE 'SNT', 'X' ; 5
2529 OF4D MESSAGE 'VAL', 'U' ; 6
2530 OF51 MESSAGE 'END', ' ' ; 7
2531 OF55 MESSAGE 'NOG', 'O' ; 8
2532 OF59 MESSAGE 'RTR', 'N' ; 9
2533 OF5D MESSAGE 'NES', 'T' ; 10
2534 OF61 MESSAGE 'NEX', 'T' ; 11
2535 OF65 MESSAGE 'FO', 'R' ; 12
2536 OF68 MESSAGE 'DIV', 'O' ; 13
2537 OF6C MESSAGE 'BR', 'K' ; 14
2538 OF6F MESSAGE 'UNT', 'L' ; 15
2539
2540 PAGE 'TELETYPE ROUTINES'
2541
2542 ; *****
2543 ; * GET CHARACTER AND ECHO IT
2544 ; *****
2545
2546 OF73 C408 GECO: LOCAL ; SET COUNT = 8
2547 OF75 CAEB LDI 8
2548 OF77 06 ST NUM(P2)
2549 OF78 DC02 CSA ; SET READER RELAY
2550 OF7A 07 CAS 2
2551 OF7B 06 $1: CSA ; WAIT FOR START BIT
2552 OF7C D420 ANI 020
2553 OF7E 9CFB JNZ $1 ; NOT FOUND
2554 OF80 C457 LDI 87 ; DELAY 1/2 BIT TIME
2555 OF82 8F04 DLY 4
2556 OF84 06 CSA ; IS START BIT STILL THERE?
2557 OF85 D420 ANI 020
2558 OF87 9CF2 JNZ $1 ; NO
2559 OF89 06 CSA ; SEND START BIT
2560 OF8A D4FD ANI X2 ; RESET READER RELAY
2561 OF8C DC01 ORI 1
2562 OF8E 07 CAS
2563 OF8F C485 $2: LDI 133 ; DELAY 1 BIT TIME
2564 OF91 8F08 DLY 8
2565 OF93 06 CSA ; GET BIT (SENSE)
2566 OF94 D420 ANI 020
2567 OF96 9804 JZ $3
2568 OF98 C401 LDI 1
2569 OF9A 9004 JMP $4
2570 OF9C C400 $3: LDI 0
2571 OF9E 9C00 JNZ $4
2572 OFA0 CAEA $4: ST TEMP(P2) ; SAVE BIT VALUE (0 OR 1)
2573 OFA2 1F RRL ; ROTATE INTO LINK
2574 OFA3 01 XAE
2575 OFA4 10 SRL ; SHIFT INTO CHARACTER
2576 OFA5 01 XAE ; RETURN CHAR TO E
2577 OFA6 06 CSA ; ECHO BIT TO OUTPUT
2578 OFA7 DC01 ORI 1
2579 OFA9 E2EA XOR TEMP(P2)
2580 OFAB 07 CAS
2581 OFAC BAEB DLD NUM(P2) ; DECREMENT BIT COUNT
2582 OFAE 9C0F $2: DLY 8 ; LOOP UNTIL 0
2583 OFB0 06 CSA ; SET STOP BIT
2584 OFB1 D4FE ANI OFE
2585 OFB3 07 CAS
2586 OFB4 8F08 DLY 8 ; DELAY APPROX. 2 BIT TIMES
2587 OFB6 40 LDE ; AC HAS INPUT CHARACTER
2588 OFB7 D4F7 ANI 07F
2589 OFB9 01 XAE
2590 OFBA 40 LDE
2591 OFBB 3F XPPC
2592 OFBC 90B5 JMP GECO ; RETURN
2593
2594 ; *****
2595 ; * PRINT CHARACTER AT TTY
2596 ; *****
2597
2598 OFBE 01 PUTC: XAE
2599 OFBF C4FF LDI 255
2600 OFC1 8F17 DLY 23
2601 OFC3 06 CSA ; SET OUTPUT BIT TO LOGIC 0
2602 OFC4 DC01 ORI 1 ; FOR START BIT. (NOTE INVERS
2603 OFC6 07 CAS
2604 OFC7 C409 LDI 9 ; INITIALIZE BIT COUNT
2605 OFC9 CAEB ST TEMP3(P2)
2606 OFCB C48A PUTC1: LDI 138 ; DELAY 1 BIT TIME
2607 OFCD 8F08 DLY 8
2608 OFCE BAEB DLD TEMP3(P2) ; DECREMENT BIT COUNT.
2609 OFD1 9810 JZ PUTC2
2610 OFD3 40 LDE ; PREPARE NEXT BIT
2611 OFD4 D401 ANI 1
2612 OFD6 CAE9 ST TEMP2(P2)
2613 OFD8 01 XAE ; SHIFT DATA RIGHT 1 BIT
2614 OFD9 1C SR
2615 OFDA 01 XAE
2616 OFDB 06 CSA ; SET UP OUTPUT BIT
2617 OFDC DC01 ORI 1
2618 OFDE E2E9 XOR TEMP2(P2)
2619 OFE0 07 CAS ; PUT BIT TO TTY
2620 OFE1 90E8 JMP PUTC1
2621 OFE3 06 CSA ; SET STOP BIT
2622 OFE4 D4FE ANI OFE
2623 OFE6 07 CAS
2624 OFE7 3F XPPC
2625 OFE8 90DA JMP PUTC ; RETURN
2626 0000 END 0

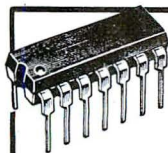
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TELETYPE ROUTINES
ADD 0335 AESTK 1050 ANDOP 05F0 AT 0C96
BEGIN 0C54 BREAK 0288 CALBIT 0080 CALLML 0963
CHEAT 007C CHEAT1 009B CHPAGE 00BA CHRNUM FFE7
CK1 0649 CKMODE 0644 CLEAR 0051 CLEAR1 0056
CLR 0C5C CMP 0562 CNP1 05C2 CNP2 05CA
CMFR 05D9 COMMA 008D DETPGE 00C1 DFAULT 0C74
DIV 0410 DO 0CCD DOLLAR 007A DOLR1 008B
DOLR2 0094 DONE 0135 DONE1 0143 DONE2 0144
DOPTR FFFF DOSTAK 107A DOUBLE 0F1C E0 0150
EOA 010D E1 0195 E10 07C6 E11 081E
E12 086D E12A 08E1 E13 0910 E14 0950
E15 097C E16 09CC E16A 0A2E E17 0A4A
E18 0AA7 E19 0B04 E2 01CC E3A 028A
E4 02DF E5 030C E6 0378 E6A 03D2
E8 064B E8A 06E5 E8B 06B2 E9 074F
END 0E05 EREH FF80 ERR 0223
ERR1 0225 ERR2 0227 EVAL 07E6
EX1 0E66 EX2 0E69 EX3 0E6B EX4 0E74
EX5 0E7D EXECIL 0076 EXPR 0E5D F1 0E80

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BRANCH TO PAGE 128



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2102-1	8080A	LM3909
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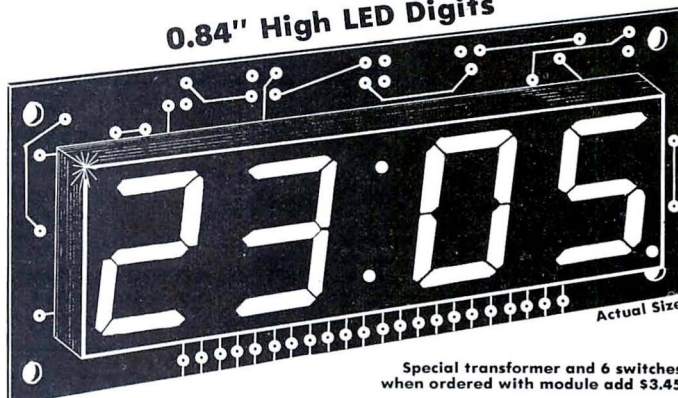
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Kit form



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4.5"	100	\$2.90
5.0"	100	\$3.00
6.0"	50	\$1.60
7.0"	50	\$1.70
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2.2/50V . . .08	.65/10	100/10V . . .10	.77/10	470/16V . . .23	1.81/10
3.3/50V . . .08	.65/10	100/10V . . .11	.85/10	470/25V . . .29	2.35/10
4.7/50V . . .08	.65/10	100/25V . . .12	1.10/10	1000/10V . .24	1.96/10
10/50V . . .08	.65/10	100/50V . . .21	1.71/10	1000/16V . .29	2.35/10
10/16V . . .08	.65/10	220/10V . . .13	1.08/10	1000/25V . .42	3.30/10
10/25V . . .08	.65/10	220/16V . . .15	1.16/10	2200/10V . .42	3.33/10
10/50V . . .10	.75/10	220/25V . . .21	1.71/10	2200/16V . .54	4.30/10
22/16V . . .08	.67/10	220/50V . . .29	2.35/10	3300/16V . .58	4.67/10
22/25V . . .09	.70/10	330/10V . . .15	1.16/10	3300/16V . .89	7.14/10
		330/16V . . .21	1.66/10		

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3.3/35V . . .12	.95/10	47/16V . . .14	1.15/10	470/16V . . .32	2.55/10
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4.7/35V . . .12	.95/10	100/10V . . .14	1.13/10	1000/16V . .39	3.15/10
4.7/50V . . .12	1.00/10	100/16V . . .17	1.30/10	1000/25V . .46	4.50/10
10/25V . . .12	1.00/10	100/25V . . .20	1.55/10	2200/10V . .50	3.96/10
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		330/10V . . .21	1.16/10		

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7411 .21	7494 .70	74195 .88	4023 .23	LM340T-6 1.25
7412 .21	7495 .70	74196 .88	4024 .84	LM340T-8 1.25
7413 .25	7496 .70	74197 .88	4025 1.14	LM340T-12 1.25
7414 .89	74100 1.28	74198 .49	4026 1.68	LM340T-15 1.25
7415 .25	74107 .30	74199 .49	4027 .40	LM340T-18 1.25
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7421 .25	74122 .44	74365 .67	4030 .23	LM3909N .69
7423 .35	74123 .61	74366 .67	4033 1.51	MC1456V 1.00
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7428 .28	74131 .88	8094 .40	4041 .79	NE540L 2.04
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7432 .25	74147 1.63	8096 .67	4043 .70	NE566A .88
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7438 .25	74151 .70	75150 1.16	4049 .40	NE562B 3.83
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7442 .53	74154 1.03	75451 .61	4051 1.26	NE566V 1.28
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1N5229B 4.3V .15 511/C	1N5229B 9.1V .15 511/C
1N5230B 4.7V .15 511/C	1N5230B 10V .15 511/C
1N5231B 5.1V .15 511/C	1N5231B 11V .15 511/C
1N5232B 5.6V .15 511/C	1N5232B 12V .15 511/C
1N5233B 6.0V .15 511/C	1N5233B 13V .15 511/C
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6-32 1/2 Screw	.75/C	4.85/M
8-32 3/8 Screw	.90/C	5.85/M
8-32 5/8 Screw	.99/C	7.00/M
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MICRODATA REALITY: Are there any other computer hobbyists using this system? If so, I'd like to say hello, swap notes and programs, etc. Would also like to know where to buy a 4- or 8-way video terminal interface card and other peripherals for Microdata Reality (Model 1600 cpu). Jack Hardman, 140 Forest Ave., Glen Ridge, NJ 07028. (201)429-8880.

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STARTING New Correspondence Exchange Club, would appreciate response from you on any useful project with a computer, visual or graphic, video camera interfacing to a computer. Any computer/printer generated pictures or posters; STARTREK, Playboy, Snoopy, Cat, any figure or design on paper. Joe Penora, 920 First Ave., Franklin Square, NY 11010.

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FOR SALE: 3 MITS 88-4mcds (4K Static) at \$150 each, 2 MITS 88-4mcd (4K dyn.) at \$190 each, 2 MITS 1K Static at \$75 each. All socketed, all work (together even) all less than 40 hrs total time. Guaranteed not assembled by a graduate engineer. JEDJ 2127 Harper, Lawrence, KS 66044. We're going from 8 to 16 bit machine!

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PDP-8 MINI COMPUTER (Straight-8) for sale or trade. Mounted in attractive walnut cabinet (wife approved for den). Complete with maintenance manual, drawings, 4K Basic, 4K Focal, Editor, PAL III assembler, Disassembler, TTY interface, games, etc., etc. Perfect condition. Free DECUS membership available for additional software. Presently in use with ASR Model 33 teletype. Can be sold with or without teletype. Sale price w/o teletype \$800.00. Rex Eagle, P.O. Box 10498, Charlotte, N.C. 28288. (704) 374-6557.

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CARD READER with documentation \$100.00 or trade. Bob Stevens, 2361 E. Foothill Blvd., Pasadena, CA 91107. (213) 449-0616.

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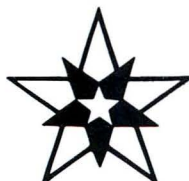
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HEX	OE54	HI	FFEE	HILINE	FF77	IF	OE46
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LST5	OE34	LSTK	FFFD	MESGS	OE37	ML	OE0E
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ZZ0053	OE03	ZZ0054	OE03	ZZ0055	OE04	ZZ0056	OE04
ZZ0057	OE08	ZZ0058	OE03	ZZ0059	OE02	ZZ005A	OE03
ZZ005B	OE05	\$0	OE2A	\$0	OE420	\$0	OE76F
\$0	OE96	\$0	OE91	\$1	OE43	\$1	OE1C6
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\$ADD1	OE8FF	\$CALB	OE800	\$CR	OE7D8	\$DOWN	OE885
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\$SKIP	OE664	\$TSTB	OE200	\$UP	OE895	\$UP1	OE8A1
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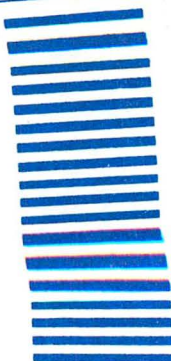
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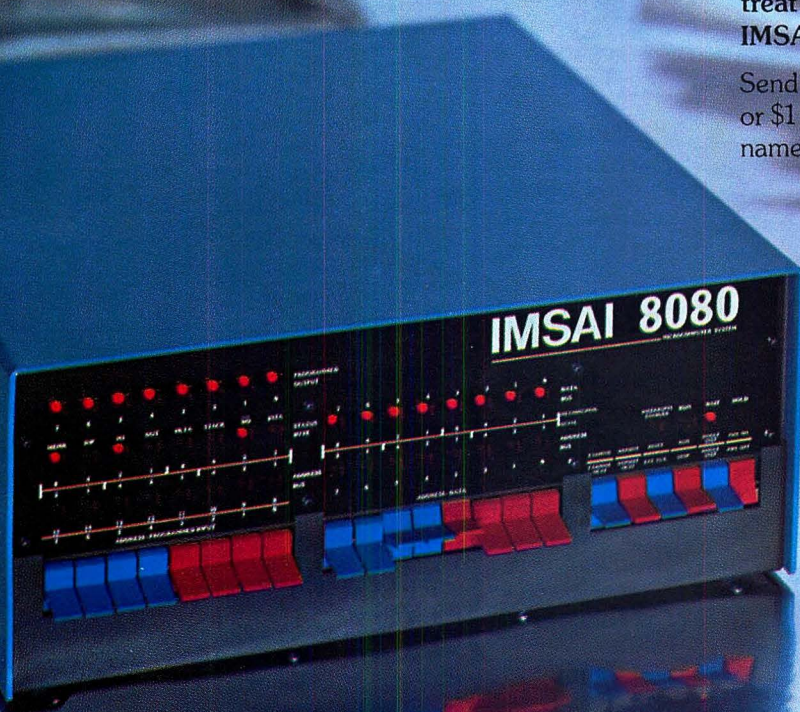
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